An On-Line BISTed SRAM IP Core

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Purpose

- To design an advanced on-line SRAM BIST IP-core for an Italtel ATM switch, satisfying strict reliability constraints.

Outline

- The target application:
  - Functionality and reliability constraints
- Implemented test strategies:
  - Data fault tolerance
  - Address fault tolerance
  - Fault latency minimization
- Conclusions.

The target memory

- Included as an IP core in an ATM switch chip unit, designed by Italtel SpA

- 0.25 µ technology
- 700 K gates of random logic
- 3.2 Mbits of RAM

Functional Constraints

- 10 K x 80 bits single-port SRAM
- 100 MHz clock frequency
- 1 memory access every 200 clock cycles

Reliability Constraints

- High fault detection of permanent (stuck-at) and transient faults (SEU, DEU, coupling) on data & addressing logic
- Fault latency < threshold imposed by the application
- Service never interrupted nor degraded
- Low area overhead.

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Vers. 1.0

6.1.1
**Problem:**
- No testing approach proved to be capable, by itself, of satisfying all the constraints

**Solution:**
- Several cooperating & concurrent test strategies

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**Proposed solution**

- On-line BIST
- Data fault tolerance
- Address fault tolerance

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- Off-line BIST
- Fault latency minimization

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**Data Fault Tolerance**

- Obtained through an on-line BIST architecture based on information redundancy:
  - Separable Hamming code: (80 + 7)-bits codeword

**Data Fault Tolerance (cont’d)**

- Detected:
  - Single & multiple stuck-at faults
  - SEUs & DEUs
  - Coupling faults
  - 7-bits burst errors
Addresses Fault Tolerance

- Errors in the addressing logic of a single block generate a 7-bits burst errors, detectable by the code.

Fault Latency Minimization

- A fault detection latency < 100 K cycles (i.e., 500 functional memory accesses) is required.
- The content of the memory must be preserved.
- No performance degradation is allowed.

Addresses Fault Tolerance (cont’d)

- Advantages:
  - No additional code-bits are required
  - Detects SEU, DEU, stuck-at & coupling in the addressing logic of a single block

Fault Latency Minimization (cont’d)

- Code-based solution implies an access-rate-related fault latency

- Off-line BIST approach to exploit the system idle time
Fault Latency Minimization (cont'd)

- The memory cells are tested sequentially
- The Cell Under Test is functionally replaced by a shadow register

Fault Latency Minimization (cont'd)

- The BIST controller tests the cell using a set of background patterns

**Conclusions**

- We presented an on-line test architecture for a single-port SRAM IP-core
- No performance degradation is introduced
- The solution has already been easily customized by Italtel to different:
  - target memories (e.g., dual ports)
  - design constraints

**Conclusions** (cont’d)

To fulfill very strict constraints imposed on safety critical RAMs, you have to resort to several concurrent test strategies.