HD²BIST: A Hierarchical Framework for BIST Scheduling, Data Patterns Delivering and Diagnosis in SoCs

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Purpose

Defining a TAM for SoC’s, capable of:

• Managing embedded cores with different test strategies (BIST’d, BIST-ready, and Scan Cores)
• Reducing routing cost
• Being compatible with (and an extension of) P1500
Goals

HD²BIST

Hierarchical Distributed Data Built In Self Test
HD$^2$-BIST

A hierarchical distributed BIST strategy for SOCs, characterized by:

- **Flexibility**
  - Test structures & methodologies
  - Test scheduling
  - TAM (control & data)

- **Reusability**
  - Horizontal vs. Vertical
A little bit of history...

- **TECS’98**: 1st idea
- **HLDVT’98**: Application to system level
- **ETW’99 + JETTA**: EDA tool for HDBIST
- **ITC’99**: Control part, only
- **ITC’00**: Data part + Industrial test cases
- ...
Outline

• Issues in Core-based systems
• HD²BIST advantages
• Experimental results
• Conclusions
Issues in Core-Based Systems:
several test strategies
Issues in Core-Based Systems:
several TAMs
Issues in Core-Based Systems:
legacy, proprietary & commercial
BIST controllers
Issues in Core-Based Systems:
hierarchy of cores
HD$^2$-BIST

The basic idea
HD²-BIST

TAP

Chip level
Test Processor

Test Pattern
Source/Sink

TAM: Test Data Bus

TAM: Test Control Bus

Wrapper

Core
HD²-BIST

Chip level
Test Processor

TAP

Test Pattern Source/Sink

Wrapper

Core

Test Pattern Source/Sink

Wrapper

Core

Test Pattern Source/Sink

Wrapper

Core
HD²-BIST

Chip level
Test Processor

Test Pattern Source/Sink

Test Pattern Source/Sink

Test Pattern Source/Sink

Wrapper

Wrapper

Wrapper

Core

Core

Core
HD^2-BIST

Chip level Test Processor

TAP

Test Pattern Source/Sink

Wrapper

Core

Test Pattern Source/Sink

Wrapper

Core

Wrapper

Core
It manages the chip-level BIST by:
- Activating BIST procedures
- Checking their statuses
- Locating failures
HD²-BIST

Chip level
Test Processor

Test Pattern Source/Sink

Wrapper

Core

Test Pattern Source/Sink

Wrapper
Description layers

- Application layer
- Token layer
- Hardware layer
Bi-directional control link:
- Forward Bus for Commands
- Backward Bus for Diagnosis
- Token-based self-checking protocols

Uni-directional data link
Hardware layer

Test Pattern Source/Sink

Wrapper

Test Chain Bus Interface

Wrapper

Core

Test Processor

Chip level

Pattern Source/Sink
Token layer

- **Command tokens**: to activate and control the test
- **Diagnosis tokens**: to notify a fault detection
Issues in Core-Based Systems: hierarchy of cores

Test Block:
• Common interface vs the core wrappers
**Issues in Core-Based Systems:**

**Test Control Bus:**
- Used to transmit *Static* Data
- **Bi-directional control link:**
  - Forward Bus for Commands
  - Backward Bus for Diagnosis and Reliability
  - Token-based self-checking protocols

**Test Data Bus:**
- Used to transmit *Dynamic* Data
- **Scan Bus Protocol**
Issues in Core-Based Systems: hierarchy of cores

Test Processor:
- Manages communications between hierarchical levels
- Implements commands from the upper level
- Acts as test data bus router
**Issues in Core-Based Systems:**

**Hierarchy of cores**

**Top Level Test Processor:**

- Manages communications at the top level
- Acts as an interface vs the TAP
**HD²BIST advantages**

The adopted architecture supports:

- *Scan-based core testing*
- *Glue-logic testing*
- *BIST-ready core management.*
Scan-based core testing

BIST’d Core

Scan Core

BIST’d Core

TB

TLTP

TAP
BIST-ready core management

BIST ready Core

TB

TP

TB

TB

BIST controller
Glue-logic testing

Scan chain of glue logic

Additional scan chain

TB₂

TB₁

TB₃

TB₄

TB₅

TP
Outline

• Issues in Core-based systems
• $\text{HD}^2\text{BIST}$ advantages
• Experimental results
• Conclusions
- Two BISTed RAMs
- Three hierarchical levels
- Tens of full-scan cores
- Combinatorial glue logic at each level

1M gates IC by LSI Logic (G11 technology)
Full scan - 7 chains
Experimental results

Test Time overhead

- Only the time to configure the ring + the latency due to the hierarchy depth

Area overhead

- NDS: 4%
- DacTOP: 3.5%
- DacTOP Plus: 3%
Test case # 2

- Part of a telecom ASIC designed by Italtel
- technology: $0.35\mu$
- glue logic: $\sim 860K$ gates
- static RAMs: 36 instances (one, two, three or four ports) for a total of 16,5 Kbits
Experimental results

Test Time overhead

- Only the time to configure the rings + time to read the test results

Area overhead

- 3%, w.r.t. the design including the BIST controllers
Conclusions

- Test Management Flexibility
- Hierarchical paradigm
- Embedded Test Oriented
- Low routing congestion
- Limited test time overhead
- Limited area overhead
- No test patterns re-computation
- Two real complex ICs have been $HD^2BIST$ed.