IEEE 1149.4 Mixed-Signal Test Bus

An overview of this new testability bus standard, along with a discussion of the architecture and how to use it.
IEEE 1149.4: Mixed-signal Test Bus Standard

- Development history
- Basic guidelines
- Test bus requirements
- Standard architecture
- Measurement example
Development History

- **September 1991**
  - Informal meeting of 15 companies in San Jose, CA
  - Draft of mission statement, objectives, request to IEEE

- **October 1991**
  - ITC meeting attracted 30 companies
  - Working Group authorized by Test Bus Steering Committee

- **Working Group meetings**
  - Since October 1991
  - Regular meetings: 3 times per year at major test events
Mission Statement

To define, document, and promote the use of a standard mixed-signal test bus that can be used at the device, sub-assembly, and system levels to improve the controllability and observability of mixed-signal designs and to support mixed-signal built-in test structures in order to reduce test development time and costs, and improve test quality.
Basic Guidelines

- Providing test bus facilities to meet the mission objectives
- Oriented toward industry: design, test, and manufacturing
- Maintaining compatibility with 1149.1 test bus features
- Coordinating with
  - IEEE 1149.1 and mainly the IEEE 1149.1B-1994
  - International industry and academic experts
Basic Guidelines

- IEEE1149.4 **does NOT** seek to
  - Solve all mixed-signal test problems
  - Dictate mixed-signal test strategies

- IEEE1149.4 **DOES** intend to
  - REDUCE the difficulty in mixed-signal testing
  - FACILITATE design-for-test
  - PROMOTE concurrent design & test approaches
Mixed-Signal Printed Circuit Assembly

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Common Defects on a mixed-signal PCA

- **Opens**
  - Z
  - Direct Connections

- **Shorts**
  - D-D
  - A-A
  - D-A

- **Missing Component**
- **Wrong Component**
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IEEE 1149.1 Boundary-Scan Architecture

CONNECTIONER

VIRTUAL TEST PROBE

PRINTED CIRCUIT ASSEMBLY

TDI
TMS
TCK
TDO
Simple, Extended and Differential Interconnects

- Analog driver
- Analog driver
- Analog driver
- Digital driver
- Differential driver (analog or digital)
- Differential receiver (analog or digital)
- Analog receiver
- Analog receiver
- Analog receiver
- Digital receiver

Extended interconnect

Simple interconnect

Differential interconnect

Single-ended transmission point

Single-ended reception point
Handling Analog Pins: Pre-1149.4

TDI: Test Data In (1149.1)
TMS: Test Mode Select (1149.1)
TCK: Test Clock (1149.1)
TDO: Test Data Out (1149.1)
DBM: Digital Boundary Module
(Boundary-Scan Cell)
Handling Analog Pins: with 1149.4

TDI: Test Data In (1149.1)
TMS: Test Mode Select (1149.1)
TCK: Test Clock (1149.1)
TDO: Test Data Out (1149.1)
DBM: Digital Boundary Module (Boundary-Scan Cell)
ABM: Analog Boundary Module
Structure of a basic 1149.4 chip (minimal config)

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Analog Boundary Module: Input Pin

- Input value can be sensed, digitised (against $V_{TH}$), and captured in the register.
- Current path into the core via AT1, AB1 and SB1.
- Ability to disconnect the receiving core from the pin using SD and drive either a 1 or a 0 (SH or SL).
- ABMs can be implemented with actual switches or can be integral in the analog circuit.
Analog Boundary Module: Output Pin

- **Dot 1 mode**
  - Logic 1/0 to output via SH/SL
  - Digital signal input capture via comparison with $V_{TH}$
  - Compatible with 1149.1 Extest, Preload/Sample

- **Analog mode**: each pin can
  - source an analog current via AB1/SB1, or
  - capture an analog voltage via SB2/AB2
  - form a current return to $V_G$ (usually ground) via SG
  - be disconnected from the core via SD
Analog Output Cell

- $V_H$ and $V_L$ allow fixed “1” and “0” values (for EXTEST) using S1, S2, S3, S4
- ATn disconnected from ABn via S5, S8
- Noise suppression via S9, S10, $V_{\text{clamp}}$ when ABn not in use

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Noise suppression via S9, S10, $V_{\text{clamp}}$ when ABn not in use.
Analog Boundary-Scan
Test of R, Measurement V1

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Test of R,  Measurement V2

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Test of R, Result

- \( R = \frac{V_2 - V_1}{I} \)

- Results for three impedances (Z1, Z2, Z3) can be calculated and checked against correct values!

- This metrology was proven and presented at the 1993 ITC by Ken Parker in a paper entitled: “Structure and Metrology for an Analog Testability Bus” by Ken Parker, John McDermid, and Stig Oresjo of HP.
IEEE 1149.4 Types of Testing

- Interconnect : Short, Open

- Parametric Testing : Passive Element measurement

- Internal Testing : DfT (Design for Test) , BIST (Built-In Self-Test)
For Further Information

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- The IEEE 1149.4 Web page:  [http://grouper.ieee.org/groups/1149/4/](http://grouper.ieee.org/groups/1149/4/)
To Learn more ....

- The IEEE Standard Document  0-7381-1755-2  SH94761-NCD;  59$
- ITC97, P8.2; IEEE D&TC, Fall 96, pp. 98-101 (Cron, Viewlogic)
- ITC93, P15.2 (Parker et al, HP); ITC96, P15.1 (Whetsel, TI); ITC96, P4.2 (Lofstrom, KLIC)
- Next events : DATE00 (Paris), VTS00 (Montreal), ITC00 (Atlantic City)