IOLTS 2008

14th IEEE
International On-Line Testing Symposium

Rodos Palace Resort, Rhodes, Greece
July 6-9, 2008
http://tima.imag.fr/conferences/iolts

Technical Program

Issues related to on-line testing are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective on-line testing techniques. These needs have increased dramatically with the introduction of very deep submicron and nanometer technologies which adversely impact noise margins and process parameters variations and make integrating on-line testing and fault tolerance mandatory in many modern ICs.

The International On-Line Testing Symposium (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The symposium also emphasizes on-line testing in the continuous operation of large applications such as wired, cellular and satellite telecommunication, as well as in secure chips. The Symposium is sponsored by the IEEE Computer Society Test Technology Technical Council and organized by TIMA Laboratory, University of Athens and University of Piraeus.
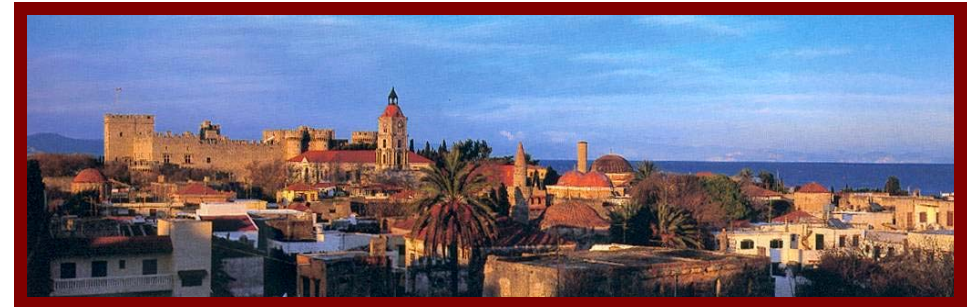
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About the location: Rhodes called from its local people the Rose of the Aegean and deserves its name because is one of the most beautiful Greek islands and one of the most popular holiday destinations in the Mediterranean. Rhodes has been famous since antiquity as the site of Colossus of Rhodes, one of the Seven Wonders of the World. The citadel of Rhodes, built by the Knights Hospitalliers, is one of the best preserved medieval towns in Europe. The ancient city of Lindos and the Valley of the Butterflies are other of the main attractions of the island.

Social Program – Excursion to Lindos and gala dinner at Rodos Palace. Lindos of Rhodes is a beautiful little village of white cubist houses at the foot of a vertical rock that is crowned by the ancient Acropolis of Lindos. The landscape all around is so barren it literally feels like a landscape from another planet. The town of Lindos itself however is perfectly located to take advantage of the two small natural harbours below and the easily defensible acropolis above it. The acropolis offers spectacular views of the surrounding harbours and coastline. Some scenes of the well-known film, The Guns of Navarone, were filmed there.

The acropolis of Lindos bares witness to the multitude of cultural influences that established themselves on the area for centuries at a time. The ancient Greek Sanctuary of Athena Lindia dominates the acropolis with the massive double-winged stoa and the massive staircase that leads to the propylaea and the temple of Athena beyond. Most of the ruins date back to the Hellenistic era and the temple of Athena Lindia was built in the 6th century BC on the spot of an earlier temple. It was destroyed by fire in 342 BC, and was built again after 300 BC along with the Propylaea and the stoa (added in 208 BC). What stands today of the sanctuary is the restoration of these Hellenistic interventions.

In Byzantine times the statue of Athena was moved to Konstantinoupolis and the church of Saint John was built at the north end of the stoa ruins. The only access point to the Acropolis in ancient times is the same one used today. A long ascent from Lindos town culminates on a small plateau right below the ruins, and from there the sacred way, a narrow and long staircase, leads to the ancient ruins atop the Acropolis.

In the medieval era, the knights surrounded the entire acropolis plateau with the impressive wall that is still visible today, and added the "Palace of the Knights" right at the top of the long staircase that leads to the acropolis. When the Turks controlled Rhodes they converted the church of St. John to a Muslim mosque and built several other edifices that were demolished when the Italians excavated the site in the 20th century.

On the acropolis of Lindos today parts of the following buildings may still be seen:
- The Doric Temple of Athena Lindia, dating from about 300 BC, built on the site of an earlier temple. Inside the temple is the table of offerings and the base of the cult statue of Athena.
- The Propylaea of the Sanctuary, also dating from the 4th century BC. A monumental staircase leads to a D-shaped stoa and a wall with five door openings.
- The Hellenistic stoa with lateral projecting wings, dating from about 200 BC. The stoa is 87 metres long and consisted of 42 columns.
- The well-known relief of a Rhodian trireme (warship) cut into the rock at the foot of the steps leading to the acropolis. On the bow stood a statue of General Hagesander, the work of the sculptor Pythokritos, who also carved the Winged Victory of Samothrace. The relief dates from about 180 BC.
- The Hellenistic staircase (2nd century BC) leading to the main archaeological area of the acropolis.
- Remains of a Roman temple, possibly dedicated to the Emperor Diocletian and dating from about 300 AD.
- The Acropolis is surrounded by a Hellenistic wall contemporary with the Propylaea and the stairway leading to the entrance to the site. A Roman inscription says that the wall and square towers were repaired at the expense of P Aelius Hagetor, the priest of Athena in the 2nd century AD.
- The Castle of the Knights of St John, built some time before 1317 on the foundations of older Byzantine fortifications. The walls and towers follow the natural conformation of the cliff. A pentagonal tower on the south side commanded the harbour, the settlement and the road from the south of the island. There was a large round tower on the east facing the sea and two more, one round and the other on a corner, on the northeast side of the enceinte. Today one of the towers at the southwest corner and one to the west survive.
- The Greek Orthodox Church of St John, dating from the 13th or 14th century and built on the ruins of a previous church, which may have been built as early as the 6th century.

10:15 – 11:35: Session 9 – Fault-Tolerance and On-Line Testing for Networks-on-Chip, Labs-on-Chip and Multiport Chips

Moderators: S.Chakravarty (LSI Logic) and B.Straube (Fraunhofer IIS/EAS)

9.1 *Communication Aware Recovery Configurations for Networks-on-Chip*, C.Rusu, C.Grecu, L.Anghel (TIMA Laboratory and University of British Columbia)

9.2 *Reliability in Application Specific Mesh-based NoC Architectures*, F.Refan, H.Alemzadeh, S.Safari, P.Prinetto, Z.Navabi (University of Tehran and Politecnico di Torino)

9.3 *On-Line Testing of Lab-on-Chip Using Digital Microfluidic Compactors*, Y.Zhao, K.Chakrabarty (Duke University)

9.4 *Self-configuration and Reachability Metrics in Massively Defective Multiport Chips*, P.Zajac, J.Collet, A.Napieralski (CNRS, University of Toulouse and Technical University of Lodz)

11:35 – 11:50: Coffee Break

11:50 – 12:50: Session 10 – Parametric Testing Techniques

Moderators: H.Stratigopoulos (TIMA) and Y.Makris (Yale University)

10.1 *Exploiting Parametric Power Supply and/or Temperature Variations to Improve Fault Tolerance in Digital Circuits*, J.Semiao, J.Freijedo, J.Rodríguez-Andina, F.Vargas, M.Bicho Dos Santos, I.Teixeira, J.P.Teixeira (IST/INESC-ID, University of Algarve, University of Vigo, Catholic University – PUCRS)

10.2 *On the detection of SSN-induced logic errors through on-chip monitoring*, F.Azais, L.Larguier, Y.Bertrand, M.Renovell (LIRMM – CNRS/University of Montpellier II)

10.3 *Guided Probabilistic Checksums for Error Control in Low Power Digital-Filters*, M.Nisar, A.Chatterjee (Georgia Institute of Technology)

12:50 – 14:00: Lunch

14:00 – 14:40: Session 11 – Radiation-Induced SER

Moderator: L.Anghel (TIMA)

11.1 *Soft-Error Vulnerability of Sub-100-nm Flip-flops*, T.Heijmen (NXP Semiconductors)

11.2 *Variation of Alpha Induced Soft Error Rate with Technology Node*, D.Leroy, R.Gaillard, E.Schaefer, C.Beltrando, S.-J.Wen, R.Wong (iRoC Technologies and Cisco)

14:40 – 14:55: Break

14:55 – 15:55: Session 12 – Self-Test Generation Techniques

Moderators: A.Salsano (Universita di Roma "Tor Vergata") and E.Simeu (TIMA)

12.1 *Deterministic Built-in TPG with Segmented FSMs*, S.Sudireddy, J.Kakade, D.Kagaris (Southern Illinois University)

12.2 *A Low-Cost Accumulator-Based Test Pattern Generation Architecture*, D.Magos, I.Voyiatzis, S.Tarnick (Technological Educational Institute of Athens, 4TECH GmbH)

12.3 *Directed Random SBST Generation for On-Line Testing of Pipelined Processors*, A.Merentitis, G.Theodorou, M.Giorgaras, N.Kranitis (University of Athens)

15:55 – 16:10: Coffee Break

16:10 – 17:10: Session 13 – Laser-Based Fault Injection in Memories

Moderators: I.Teixeira (IST/INESC-ID) and R.Velazco (TIMA)

13.1 *SDRAM Architecture & Single Event Effects revealed with Laser*, A.Bougerol, F.Miller, N.Buard (EADS)

13.2 *Detailed analyses of single laser shot effects in the configuration of a Virtex-II FPGA*, G.Canivet, J.Clediere, J.-B.Ferron, F.Valette, M.Renaudin, R.Leveugle (TIMA Laboratory, CESTI/CEA-LETI, DGA/CELAR and Tiempo)

13.3 *Dynamic testing of an SRAM-based FPGA by time-resolved laser fault injection*, V.Pouget, A.Douin, G.Foucard, P.Peronnard, D.Lewis, P.Fouillat, R.Velazco (IMS – University of Bordeaux and TIMA Laboratory)

17:10 – 17:30: Closing Remarks

08:00 – 09:00: Tutorial Registration

09:00 – 17:00: Test Technology Educational Program (TTEP) 2008 Full-Day Tutorial
Soft Errors: Technology Trends, System Effects, Protection Techniques and Case Studies
S.Mitra (Stanford University), P.Sanda (IBM), N.Seifert (Intel)

16:00 – 18:00: Symposium Registration

Monday July 7 2008

08:00 – 09:00: Symposium Registration

09:00 – 10:00: Opening Session
09:00 – 09:15: Welcome Message
M.Nicolaidis (TIMA Laboratory), A.Paschalis (University of Athens), *General Chairs*
D.Gizopoulos (University of Piraeus), N. Seifert (Intel), *Program Chairs*
09:15 – 10:00: Keynote Talk
Emerging Trends in Complex System-Chips and their Implications on Yield
Yervant Zorian, VP/Chief Scientist (Virage Logic)

10:00 – 10:15: Break

10:15 – 11:15: Session 1 – On-Line Error Detection and Correction

Moderators: C.Landrault (LIRMM) and J.Collet (LAAS)

1.1 *On-Line Failure Detection and Confinement in Caches*, J.Abella, P.Chaparro, X.Vera, J.Carretero, A.González (Intel Barcelona Research Center)

1.2 *An Enhanced Logic BIST Architecture for Online Testing*, F.Yang, S.Chakravarty, N.Devta-Prasanna, S.M.Reddy and I.Pomeranz (University of Iowa, LSI Corporation and Purdue University)

1.3 *Design Techniques for Bit-Parallel Galois Field Multipliers with Online Single Error Correction and Double Error Detection*, J.Mathew, A.Jabir, D.Pradhan (University of Bristol and Oxford Brookes University)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 2 – Self-Checking Circuits and Error Detecting Codes

Moderators: Z.Peng (Linköping U.) and R.Parekhji (Texas Instruments India)

2.1 *Verification and Analysis of Self-Checking Properties through ATPG*, M.Hunger, S.Hellebrand (University of Paderborn)

2.2 *Physical Demonstration of Polymorphic Self-checking Circuits*, R.Ruzicka, L.Sekanina, R.Prokop (Brno University of Technology)

2.3 *New Linear SEC-DED Codes with Reduced Triple Bit Error Miscorrection Probability*, M.Richter, K.Oberlaender, M.Goessel (University of Potsdam and Infineon AG)

12:30 – 13:30: Lunch

13:30 – 14:30: Special Session 1 – Radiation Hardening Techniques

Organizer: N.Seifert (Intel) – Moderator: C.Papachristou (Case Western Res. University)

S1.1 *Soft Error Protection Techniques*, S.Mitra (Stanford University)

S1.2 *Growing Interest of Advanced Commercial CMOS Technologies for Space and Medical Applications. Illustration with a New Nano-Power and Radiation-Hardened SRAM in 130nm CMOS*, P.Roche, M.Lysinger, G.Gasiot, M.Zamanian, P.Dautriche (STMicroelectronics)

S1.3 *Soft Error Rates of Hardened Sequentials utilizing Local Redundancy*, N.Seifert (Intel)

14:30 – 14:45: Break

14:45 – 15:45: Session 3 – Soft Error Detection and Correction Methodologies

Moderators: S.Hellebrand (University of Paderborn) and N.-E.Zergainoh (TIMA)

3.1 *False Error Study of On-Line Soft Error Detection Mechanisms*, K.Kumar Reddy, B.Amrutur, R.Parekhji (Indian Institute of Science and Texas Instruments India)

3.2 *Integrating Scan Design and Soft Error Correction in Low-Power Applications*, M.Imhof, H.-J.Wunderlich, C.Zoellin (University of Stuttgart)

3.3 *A Built-In Self-Test Scheme for Soft Error Rate Characterization*, A.Sanyal, S.Alam, S.Kundu (University of Massachusetts and Freescale)

15:45 – 16:00: Coffee Break

16:00 – 17:00: Session 4 – Control-Flow Checking and Fault-Tolerance in Special Applications
Moderators: E.Boehl (Robert Bosch GmbH) and M.Benabdenbi (University of Paris 6)
4.1 *Budget-dependent control flow error detection*, R.Vemu, J.Abraham (University of Texas at Austin)
4.2 *Software Self-Testing of a Symmetric Cipher with Error Detection Capability*, P.Maistri, C.Excoffon, R.Leveugle (TIMA Laboratory)
4.3 *A Fault-Tolerant Attitude Determination System based on COTS Devices*, R.Duarte, L.Martins-Filho, G.Knop, R.Prado (Federal University of Ouro Preto, Federal University of ABC and Federal Center of Technological Education)

17:00 – 17:15: Break

17:15 – 17:55: Session 5 – Fault Injection
Moderator: A.Chatterjee (Georgia Tech.) and M.Psarakis (University of Piraeus)
5.1 *A New Approach for Transient Fault Injection using Symbolic Simulation*, A.Darbari, B.Al-Hashimi, P.Harrod, D.Bradley (University of Southampton and ARM)
5.2 *SystemC-based Minimum Intrusive Fault Injection Technique with Improved Fault Representation*, R.Shafik, P.M.Rosinger, B.Al-Hashimi (University of Southampton)

17:55 – 18:00: Break

18:00 – 19:00: Special Session 2 – Benchmarking and Standardization in Software-Based SER Characterization: Towards an IEEE Task Force?
Organizer/Moderator: M.Nicolaidis (TIMA Laboratory)
Co-organizers: D.Alexandrescu (iRoC, algorithms and software issues), L.Anghel (TIMA, academia liaison), S.Bhabu (Cadence, EDA issues), R.Parekhji (TI, Design issues), N.Seifert (Intel, Technology issues), S.-J.Wen (CISCO, Systems issues), Y.Zorian (Virage Logic, IP issues)
Co-organized by the On-line Testing TAC of the IEEE Computer Society TTTC

20:00: Welcome Reception

Tuesday July 8 2008

09:00 – 09:45: Invited Talk
Systematical Method of Quantifying SEU FIT
ShiJie Wen, Si Technologist (Cisco Component Engineering), Dan Alexandrescu (iRoC)

09:45 – 10:00: Break

10:00 – 11:20: Session 6 – Mitigation Techniques for Transient Errors
Moderators: E.Ibe (Hitachi) and M.Sonza Reorda (Politecnico di Torino)
6.1 *Using Low Pass Filters in Mitigation Techniques against Single Event Transients in 45nm-technology LSIs*, T.Uemura, R.Tanabe, Y.Tosaka, and S.Satoh (Fujitsu Labs)
6.2 *On the Minimization of Potential Transient Errors and SER in Logic Circuits Using SPFD*, S.Almukhaizim, Y.Makris, Y.-S.Yang, A.Veneris (Kuwait University, Yale University and University of Toronto)
6.3 *Propagation of Transients Along Sensitizable Paths*, S.Gangadhar, M.Skoufis, S.Tragoudas (Southern Illinois University)
6.4 *On the Evaluation of Radiation-induced Transient Faults in Flash-based FPGAs*, N.Battezzati, S.Gerardin, A.Manuzzato, A.Paccagnella, S.Rezgui, L.Sterpone, M.Violante (Politecnico di Torino, University of Padova and Actel)

11:20 – 11:35: Coffee Break

11:35 – 12:35: Session 7 – Memory Self-Test and Self-Repair
Moderators: P.Girard (LIRMM) and M.Violante (Politecnico di Torino)
7.1 *A Hybrid Approach to the Test of Cache Memory Controllers Embedded in SoCs*, W.Perez, J.Velasco-Medina, D.Ravotto, E.Sanchez, M.Sonza Reorda (Universidad del Valle, Colombia and Politecnico di Torino, Italy)

7.2 *A BISR Architecture for Embedded Memories*, K.Z.Pekmestzi, N.Axelos, I.Sideris, N.Moshopoulos (National Technical University of Athens)
7.3 *Embedding Current Monitoring in H-Tree RAM Architecture for Multiple SEU Tolerance and Reliability Improvement*, C.Argyrides, F.Vargas, M.Moraes, D.Pradhan, (Bristol University and Catholic University - PUCRS)

12:35 – 13:45: Lunch

13:45 – 14:45: Special Session 3 – Panel: SER in Automotive: what is the impact of the AEC Q100-G spec?
Organizer/Moderator: T.Heijmen (NXP)
Panelists: F.Vermunt (NXP Semiconductors), E.Ibe (Hitachi), P.Roche (ST Microelectronics), A.Bougerol (EADS)

14:45 – 15:45: Session 8 – Posters
8.1 *Yield Improvement, Fault-Tolerance to the Rescue?*, J.Vial, A.Bosio, P.Girard, C.Landrault, S.Pravossoudovitch, A.Virazel (LIRMM)
8.2 *Smart Hardening for Round-based Encryption Algorithms: Application to Advanced Encryption Standard*, C.Lopez-Ongil, A.Jimenez-Horas, M.Portela-Garcia, M.Garcia Valderas, E.San Millán, L.Entrena (Universidad Carlos III de Madrid)
8.3 *SRAM cell design protected from SEU upsets*, Y.Shiyanovskii, F.Wolff, C.A.Papachristou (Case Western Reserve University)
8.4 *A Modular Memory BIST for Optimized Memory Repair*, P.Oehler, A.Bosio, G.Di Natale, S.Hellebrand (University of Paderborn and LIRMM)
8.5 *A Novel GA-Based High-Level Synthesis Technique To Enhance RT-Level Concurrent Testing*, N.Karimi, S.Aminzadeh, S.Safari, Z.Navabi (University Of Tehran)
8.6 *A New Radiation Hardened By Design Latch for Ultra-Deep-Sub-Micron Technologies*, Z.Huang, H.Liang (Hefei University of Technology)
8.7 *Basic Architectures for Logic Self Repair*, H.Vierhaus, T.Koal (BTU Cottbus)
8.8 *Developing Fault Injection Environment for Complex Experiments*, P.Gawkowski, J.Sosnowski (Warsaw Technical University)
8.9 *Development of a Testbench for Validation of DMT and DT2 Fault-Tolerant Architectures on SOI PowerPC7448*, M.Pignol, T.Parrain, V.Claverie, C.Boleat, G.Estaves (CNES, Delta Technologies Sud-Ouest, Alten Sud-Ouest, Astrium SAS and Thales Alenia Space)
8.10 *Dynamic scheduling of test routines for efficient online self-testing of embedded microprocessors*, N.Bartzoudis, V.Tantsios, K.Mcdonald-Maier (Centre Tecnològic de Telecomunicacions de Catalunya and University of Essex)
8.11 *Fault Tolerant Reversible Finite Field Arithmetic Circuits*, J.Mathew, J.Singh, A.Abu Taleb, D.Pradhan (University of Bristol)
8.12 *On Line Testing of Single Feedback Bridging Fault in Cluster Based FPGA by Using Asynchronous Element*, N.Das, P.Roy, H.Rahaman (Bengal Engg. & Science University, Shibpur and Marine Engineering and Research Institute, Kolkata)
8.13 *Totally Fault Tolerant RNS based FIR Filters*, S.Pontarelli, G.Cardarilli, M.Re, A.Salsano (University of Rome -Tor Vergata and Italian Space Agency)

16:00: Social Event (Tour and Gala Dinner)

Wednesday July 9 2008

09:00 – 10:00: Special Session 4 – Reliability and Circuit Simulation
Organizer: R.Aitken (ARM) – Moderator: S.Mitra (Stanford University)
S4.1 *Modeling and Simulation of Circuit Aging in Scaled CMOS Design*, Y.Cao (Arizona State U.)
S4.2 *Design Solution and Flow for reliability in Advanced Cmos technologies*, J.-P.Geronimi (ST Microelectronics)
S4.3 *Tool-independent Reliability Simulation*, T.Heijmen (NXP)

10:00 – 10:15: Break