IOLTS 2009

15th IEEE International On-Line Testing Symposium

Sesimbra Hotel & Spa Resort, Sesimbra-Lisbon, Portugal

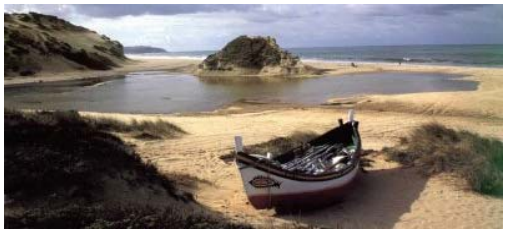
June 24-26, 2009

http://www-tima.imag.fr/conferences/iolts

Technical Program

Issues related to on-line testing are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective on-line testing techniques. These needs have increased dramatically with the introduction of very deep submicron and nanometer technologies which adversely impact noise margins, process, voltage and temperature variations, aging and wearout and make integrating on-line testing and fault tolerance mandatory in many modern ICs.

The International On-Line Testing Symposium (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The symposium also emphasizes on-line testing in the continuous operation of large applications such as wired, cellular and satellite telecommunication, as well as in secure chips. The Symposium is sponsored by the IEEE Computer Society Test Technology Technical Council and organized by TIMA Laboratory, INESC-ID, and University of Piraeus.



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About the location: Sesimbra is a tiny fishing village in a sheltered bay overlooked by a Moorish castle that also encloses a 12th century church and affords wonderful views from its ramparts. In the old town is a 17th century fort overlooking the sea, a good starting point for a scenic walk before hitting the beach that, although crowded in the summer, has unpolluted waters ideal for swimming. In late afternoon the fishing boats return and there's a fish auction on the dockside. That same fresh fish can be sampled at one of the several restaurants along the shore. A short drive or a 30-minute bus journey from Sesimbra leads to windswept Cabo Espichel, quite a mystical and eerie cape. The views of the coast and ocean are stunning, with cliffs dropping almost vertically several hundred feet into the Atlantic. In such a dramatic and pristine setting, it is not surprising that large dinosaur footprints were found nearby on Lagosteiros Beach.

About the Venue: IOLTS 2009 will be held in Sesimbra Hotel & SPA, one of the Finest Resorts of the area. The hotel is located in a long beach with warm and calm waters 30km south of Lisbon. Portugal's capital is famous for its monuments, museums and rich cultural life. Although it boasts a range of must-see sights, its biggest pleasures are its streetlife and setting, admired from a pavement cafe or simply by wandering around the atmospheric old quarters.

Social Program: The irresistible call of the sea takes us to the submarine wonders revealed by Apnea, a boat with the hull in glass that the French Joseph Bridel operates with his son, François Bridel. Five years ago they created the Aquarama company, purchased this "floating submarine" and launched into the sea in the wonderful coastline of Sesimbra. The Apnea is different and special due to its transparent hull that provides panoramic views of the ocean depths. The cruise departs from "Porto de Abrigo", in Sesimbra, and goes to "Praia do Inferno" (the beach of Hell), before "Espichel" Cape. There are three small rooms on the ground floor, where you can dive in the Atlantic without even wetting the feet. After all, is this view, below the waterline, that distinguishes the Apnea of other cruises.

4.2 *Enhanced Self-Configurability and Yield in Multicore Grids*, E.Kolonis, M.Nicolaidis, D.Gizopoulos, M.Psarakis, J.Collet, P.Zajac (University of Piraeus, TIMA Lab, and LAAS)
4.3 *Online Error Detection and Correction of Erratic Bits in Register Files*, X.Vera, J.Abella, J.Carretero, P.Chaparro, A.Gonzalez (Intel Barcelona Research Center)

15:45 – 16:00: Coffee Break

16:00 – 17:00: Session 5 – Soft Errors and FPGAs

Moderator: R.Velazco (TIMA Lab)
5.1 *Application-oriented SEU sensitiveness analysis of Atmel rad-hard FPGAs*, N.Battezzati, F.Decuzzi, M.Violante, M.Briet (Politecnico di Torino and Atmel Corporation)
5.2 *Exploiting Embedded FPGA in On-line Software-based Test Strategies for Microprocessor Cores*, M.Grosso, M.Sonza Reorda (Politecnico di Torino)
5.3 *Evaluating Large Grain TMR and Selective Partial Reconfiguration for Soft Error Mitigation in SRAM-based FPGAs*, J.R.Azambuja, F.Sousa, L.Rosa, F.Kastensmidt (UFRGS)

17:00 – 17:15: Break

17:15 – 18:15: Session 6 – Memories SEU Tolerance and Characterization

Moderator: M.Portela-Garcia (University Carlos III de Madrid)
6.1 *Novel DRAM Mitigation Technique*, A.Bougerol, F.Miller, N.Buard (EADS)
6.2 *SRAM Cell Design using Tri-state Devices for SEU Protection*, Y.Shiyanovskii, F.Wolff, C.Papachristou (Case Western Reserve University)
6.3 *Critical Charge Characterization in 6-T SRAMs During Read Mode*, S.Bota, G.Torrens, B.Alorda, J.Segura (Universitat de les Illes Balears)

18:15 – 18:30: Break

18:30 – 19:30: Special Session 1 – Panel: Realistic Low Power Design: Let Errors Occur and Correct them Later or Mitigate Errors via Design Guardbanding and Process Control?

Organizer/Moderator: A.Chatterjee (Georgia Tech.)
Panelists: J.Abraham (U. of Texas at Austin), A.Singh (Auburn U.), E.Maricau (KU Leuven), R.Kumar (U. of Illinois at Urbana-Champaign), C.Papachristou (Case Western Reserve U.)

20:00: Welcome Reception

Thursday June 25 2009

09:00 – 10:00: Session 7 – Soft Errors Tolerance

Moderator: E.Ibe (Hitachi)
7.1 *A Fast Error Correction Technique for Matrix Multiplication Algorithms*, C.Argyrides, D.Pradhan, C.Lisboa, L.Carro (University of Bristol and UFRGS)
7.2 *Soft Error Detection and Correction for FFT Based Convolution using Different Block Lengths*, P.Reviriego, J.A.Maestro, A.O'Donnell, C.Bleakley (Universidad Antonio de Nebrija and University College Dublin)
7.3 *In-depth Analysis of Digital Circuits against Soft Errors for Selective Hardening*, M.Garcia Valderas, M.Portela-Garcia, C.Lopez-Ongil, L.Entrena (Universidad Carlos III de Madrid)

10:00 – 10:15: Break

10:15 – 11:15: Special Session 2 – Design for Reliability and Dependability Issues in Massively Parallel Processor Chips

Organizers: N. Zergainoh (TIMA Lab), D.Gizopoulos (University of Piraeus)
Moderator: J.Abraham (University of Texas at Austin)
S2.1 *DFx for Massively Multi-Processors*, X.Vera (Intel Barcelona Research Center)
S2.2 *Designing Dependable Multicore Systems with Unreliable Components*, V.Chandra (ARM)
S2.3 *Variability and Reliability-Aware Application tasks scheduling and power control (Voltage and Frequency Scaling) in the future Nanoscale Chip Multiprocessors*, G.Bizot, N.Zergainoh, and M.Nicolaidis (TIMA Lab, UJF-CNRS-INPG, University of Grenoble)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 8 – Coding Techniques

Moderator: C.Papachristou (Case Western Reserve University)
8.1 *Concurrent Checking with Split-Parity Codes*, M.Richter, M.Goessel (University of Potsdam)
8.2 *Multilinear Codes for Robust Error Detection*, Z.Wang, M.Karpovsky, B.Sunar (Boston University and Worcester Polytechnic Institute)
8.3 *Fault Tolerance in 2-D Discrete Wavelet Lifting Transforms*, S.-H.Hu, J.Abraham (Freescale Semiconductor and University of Texas)

12:30 – 13:30: Lunch

13:30 – 14:30: Special Session 3 – High Altitude and Remote SEU Experiments

Organizer: R.Velazco (TIMA Lab)
Moderator: M.Sonza Reorda (Politecnico di Torino)
S3.1 *Highs and Lows of Radiation Testing*, D.Alexandrescu, A.Lhomme-Perrot, E.Schaefer, C.Beltrando (iRoC Technologies)
S3.2 *A generic platform for remote accelerated tests and high altitude SEU experiments on advanced ICs: correlation with MUSCA SEP3 calculations*, G.Hubert, R.Velazco and P.Peronnard (ONERA-CERT, TIMA Lab)
S3.3 *Using Test Infrastructures for (remote) Online Evaluation of the Sensitivity to SEUs of FPGAs*, A.V.Fidalgo, G.R.Alves, M.C.Felgueiras, M.G.Gericota (ISEP Porto)

14:30 – 15:30: Session 9 – Posters

9.1 *Briefing Power/Reliability Optimization in Embedded Software Design*, F.Vargas, M.Portela-Garcia, C.Lopez-Ongil, M.Garcia Valderas, L.Entrena (Catholic University – PUCRS, Universidad Carlos III de Madrid)
9.2 *Linear and Nonlinear MISR Operations for Safety and Security in Automotive Applications*, P.Duplys, E.Boehl (Robert Bosch GmbH)
9.3 *FPGA-based Testing Strategy for Cryptographic Chips: A Case Study on Elliptic Curve Processor for RFID Tags*, J.Fan, D.Karaklajić, M.Knezevic, R.Maes, V.Rozic, L.Batina, I.Verbauwhede (K. U. Leuven)
9.4 *Error detection in addition chain based ECC point multiplication*, S.Pontarelli, G.Cardarilli, M.Re, A.Salsano (University of Rome –"Tor Vergata")
9.5 *Detectability Analysis of Small Delays Due to Resistive Opens Considering Process Variations*, J.Garcia-Gervacio, V.Champac (INAOE)
9.6 *Controllability and Observability in Mixed Signal Cores*, J.Da Rocha, N.Dias, A.Neves, G.Santos, A.Monteiro, M.Santos, J.P.Teixeira (IST/INESC-ID, SiliconGate and Lisboa Technical University)
9.7 *A fault tolerant journalized stack processor architecture*, A.Ramazani, M.Amin, F.Monteiro, C.Diou, A.Dandache (LICM and University of Metz)
9.8 *Pseudo-Random Number Generation Applied to Robust Modern Cryptography: A New Technique for Block Ciphers*, A.Jimenez-Horas, E.San Millan, C.Lopez-Ongil, M.Portela-Garcia, M.Garcia Valderas, L.Entrena (Universidad Carlos III de Madrid)
9.9 *An Input Vector Monitoring Concurrent BIST scheme Exploiting "X" values*, I.Voyiatzis, D.Gizopoulos, A.Paschalis (TEI of Athens, University of Piraeus and University of Athens)
9.10 *Analysis of the Extra Delay on Interconnects Caused by Resistive Opens and Shorts*, J.Rius, P.Maqueda (UPC)
9.11 *C-testable S-box Implementation for Secure Advanced Encryption Standard*, H.Rahaman, J.Mathew, D.Pradhan (Bengla University and University of Bristol)
9.12 *Fault Tolerance Evaluation of a Synchronous NoC Router Based on Fault Injection*, A.Eghbal, P.M.Yaghini, H.Pedram, H.R.Zarandi (Amirkabir University of Technology and Sharif University of Technology)

16:00: Social Event (Tour and Gala Dinner)

Friday June 26 2009

08:30 – 09:15: Keynote Talk

Accessing Embedded Instruments Online: A Vision based on IJTAG, Jeff Rearick, AMD Fellow

09:15 – 09:30: Break

09:30 – 10:30: Session 10 – Fault-Tolerance Techniques

Moderator: P.Girard (LIRMM)

10.1 *A Low Cost Fault-Tolerant Technique for Carry Look-Ahead Adder*, A.Namazi, A.Ejlali, S.Miremadi (Southampton University and Sharif University of Technology)

10.2 *Delay-Fault Tolerance to Power Supply Voltage Disturbances Analysis in Nanometer Technologies*, J.Semiao, J.Freijedo, J.J. Rodriguez-Andina, F.Vargas, M.Santos, I.Teixeira, J.P.Teixeira (University of Algarve, University of Vigo, Catholic University – PUCRS, IST/INESC-ID and Lisboa Technical University)

10.3 *Designing Fault Tolerant FSM by Nano-PLA*, S.Baranov, I.Levin, O.Keren, M.Karpovsky (Bar Ilan University, Tel Aviv University and Boston University)

10:30 – 10:45: Coffee Break

10:45 – 11:45: Session 11 – Field Testing and Self-Adaptation

Moderator: H.Stratigopoulos (TIMA Lab)

11.1 *Design Techniques and Tradeoffs in Implementing Non-destructive Field Test Using Logic BIST Self-Test*, M.Shah, A.Dutta, S.Gangasani, R.Parekhji (Texas Instruments India)

11.2 *On-Line Characterization and Reconfiguration for Single Event Upset Variations*, K.Zick, J.Hayes (University of Michigan)

11.3 *Aggressively Voltage Overscaled Adaptive RF Systems Using Error Control at the Bit and Symbol Levels*, J.Natarajan, A.Chatterjee (Georgia Institute of Technology)

11:45 – 12:00: Break

12:00 – 13:00: Session 12 – Encoders, Checkers and Fault Secureness

Moderator: A.Bystrov (University of Newcastle)

12.1 *An Effective Fast and Small-Area Parallel-Pipeline Architecture for OTM-Convolutional Encoders*, H.Jaber, F.Monteiro, A.Dandache (University of Metz)

12.2 *Ultra Low Cost Asynchronous Handshake Checker*, S.Zeidler, M.Ehrig, M.Krstic, C.Wolf, R.Kraemer (IHP Microelectronics)

12.3 *ATPG-Based Grading of Strong Fault-Secureness*, M.Hunger, S.Hellebrand, A.Czutro, I.Polian, B.Becker (University of Paderborn and University of Freiburg)

13:00 – 13:15: Symposium Closing Remarks

13:15 – 14:00: Lunch

13:30 – 14:00: Tutorial Registration

14:00 – 20:00: Test Technology Educational Program (TTEP) 2009 Tutorial
Parameter Variations and Self-Calibration/Self-Repair Solutions in Nanometer Technologies

S.Mukhopadhyay (Georgia Institute of Technology), R.Rao (IBM T.J.Watson Research Center), P.Elakkumanan (IBM Semiconductor R&D Center), S.Bhunia (Case Western Reserve University)

Tuesday June 23 2009

16:00 – 18:00: Symposium Registration

Wednesday June 24 2009

07:30 – 09:00: Symposium Registration

09:00 – 10:00: Opening Session

09:00 – 09:15: Welcome Message

M.Nicolaidis (TIMA Laboratory), M.Santos (INESC-ID), *General Chairs*
D.Gizopoulos (University of Piraeus), A. Chatterjee (Georgia Tech), *Program Chairs*

09:15 – 10:00: Keynote Talk

Trusted ILLIAC: A Configurable Hardware Framework for Application-Aware Reliability and Security, Ravishankar Iyer, Professor, University of Illinois at Urbana-Champaign

10:00 – 10:15: Break

10:15 – 11:35: Session 1 – Aging Monitoring and Analysis

Moderator: J.Hayes (University of Michigan)

1.1 *Aging Analysis of Circuit Timing Considering NBTI and HCI*, D.Lorenz, G.Georgakos, U.Schlichtmann (TU München and Infineon)

1.2 *Built-In Aging Monitoring for Safety -Critical Applications*, J.Vazquez, A.Ziesemer Jr., I.Teixeira, M.Santos, J.P.Teixeira, V.Champac, R.Reis (INAOE, UFRGS, INESC-ID)

1.3 *An I-IP Based Approach for the Monitoring of NBTI Effects in SoCs*, C.Guardiani, A.Shibkov, A.Brambilla, G.Storti Gajani, D.Appello, F.Piazza and P.Bernardi (ST Microelectronics, Politecnico di Torino, Elite, Politecnico di Milano)

1.4 *A Methodology for Measuring Time-Dependent Transistor Degradation Effects Towards Accurate Reliability Simulation*, E.Maricau, G.Gielen (KU Leuven)

11:35 – 11:45: Coffee Break

11:45 – 12:45: Session 2 – Transient Faults Evaluation and Analysis

Moderator: E.Cota (UFRGS)

2.1 *Comparing Transient-Fault Effects on Synchronous and on Asynchronous Circuits*, R.Possamai Bastos, Y.Monnet, G.Sicard, F.Kastensmidt, M.Renaudin, R.Reis (UFRGS, Tiempo, TIMA Lab)

2.2 *Invariant Checkers: an Efficient Low Cost Technique for Run-time Transient Errors Detection*, C.Grando, C.Lisboa, A.Moreira, L.Carro (UFRGS)

2.3 *Toward Automated Fault Pruning with Petri Nets*, P.Maistri, R.Leveugle (TIMA Lab)

12:45 – 13:30: Lunch

13:30 – 14:30: Session 3 – System-Level Reliability and Security

Moderator: I.Polian (University of Freiburg)

3.1 *A Low-Cost Solution for Developing Reliable Linux-based Space Computers for On-Board Data Handling*, M.Violante, L.Esposti (Politecnico di Torino and Thales Alenia Space)

3.2 *Nonlinear Compression Functions using the MISR Approach for Security Purposes in Automotive Applications*, E.Boehl, P.Duplys (Robert Bosch GmbH)

3.3 *Improving Yield of Torus NoCs Through Fault- Diagnosis-and-Repair of Interconnect Faults*, C.Concatto, P.Almeida, F.Kastensmidt, E.Cota, M.Lubaszewski, M.Hervé (UFRGS)

14:30 – 14:45: Break

14:45 – 15:45: Session 4 – Microprocessors and Multiprocessors

Moderator: A.Paschalis (University of Athens)

4.1 *Evaluating Alpha-induced Soft Errors in Embedded Microprocessors*, P.Rech, S.Gerardin, A.Paccagnella, P.Bernardi, M.Grosso, M.Sonza Reorda, D.Appello (University of Padova, Politecnico di Torino, and ST Microelectronics)