# 16th IEEE International On-Line Testing Symposium

Chandris Hotel, Corfu Island, Greece
July 5-7, 2010
http://tima.imag.fr/conferences/iolts

# Final Technical Program

## Monday July 5, 2010

**07:30 – 09:00: Symposium Registration**

**09:00 – 10:00: Opening Session**

**09:00 – 09:15: Welcome Message**

M.Nicolaidis (TIMA Lab), A.Paschalis (U Athens), *General Chairs*
D.Gizopoulos (U Piraeus), A.Chatterjee (Georgia Tech), *Program Chairs*

**09:15 – 10:00: Keynote Talk I**

*Industrial Impacts of SER on Today's Consumer Electronic Arenas*,
Philippe Roche (ST Microelectronics)

**10:00 – 10:15: Break**

**10:15 – 11:35: Session 1 – Degradation Modeling and Monitoring**

Moderators: P.Girard (LIRMM) and C.Slayman (Ops A La Carte)

1.1 *A Self-Consistent Model to Estimate NBTI Degradation and a Comprehensive On-Line System Lifetime Enhancement Technique*, G.Karakonstantis, C.Augustine, K.Roy (Purdue University)
1.2 *Predictive Error Detection by On-line Aging Monitoring*, J.Vazquez, V.Champac, A.Ziesemer Jr., R.Reis, J.Semiao, I.Teixeira, M.Santos, J.P.Teixeira (INESC-ID, INAOE, UFRGS, U. Algarve, IST/UTL)
1.3 *Temperature Dependence of NBTI Induced Delay*, S.Khan, S.Hamdioui (Delft U.)
1.4 *Aging Test Strategy and Adaptive Test Scheduling for SoC Failure Prediction*, H.Yi, T.Yoneda, M.Inoue, Y.Sato, S.Kajihara, H.Fujiwara (Nara Institute of Science and Technology, Kyusyu Institute of Technology, and Japan Science and Technology Agency)

**11:35 – 11:50: Coffee Break**

**11:50 – 12:50: Session 2 – Transients Analysis and Evaluation**

Moderators: R.Velazco (TIMA Lab) and T.Inoue (Hiroshima U.)

2.1 *Analysis of Root Causes of Alpha Sensitivity Variations on Microprocessors Manufactured using Different Cell Layouts*, P.Rech, M.Grosso, F.Melchiori, D.Loparco, D.Appello, L.Dilillo, A.Paccagnella, M.Sonza Reorda (LIRMM, Politecnico di Torino, ST Microelectronics, U. Padova)
2.2 *Evaluating Transient-Fault Effects on Traditional C-element's Implementations*, R.Possamai Bastos, G.Sicard, F.Kastensmidt, M.Renaudin, R.Reis (TIMA Lab, UFRGS, TIEMPO)
2.3 *Probabilistic Methods for the Impact of an SET in Combinational Logic*, S.Gangadhar, S.Tragoudas (Southern Illinois U Carbondale)

**12:50 – 14:00: Lunch**

**14:00 – 15:00: Session 3 – Multicore/Manycore On-Line Testing**

Moderators: M.Sonza Reorda (Politecnico di Torino) and R.Kumar (U. Illinois at Urbana-Champaign)

3.1 *Analysis of On-Line Self-Testing Policies for Real-Time Embedded Multiprocessors in DSM Technologies*, O.Heron, J.Guilhemsang, N.Ventroux, A.Giulieri (CEA LIST, and LEAT)
3.2 *Distributed Online Software Monitoring of Manycore Architectures*, E.Faure, M.Benabdendi, F.Pêcheux (LIP6, U Pierre and Marie Curie, TIMA Lab)

3.3 *SBST for On-Line Detection of Hard Faults in Multiprocessor Applications Under Energy Constraints*, A.Merentitis, D.Margaris, N.Kranitis, A.Paschalis, D.Gizopoulos (U Athens and U Piraeus)

**15:00 – 15:15: Break**

**15:15 – 16:15: Session 4 – Analog and Mixed-Signal Circuit Testing**

Moderators: M.Lubaszewski (U. Federal do Rio Grande do Sul) and P.Fouillat (IXL-ENSEIRB)

4.1 *An Analog VLSI Multilayer Perceptron and its Application Towards Built-In Self-Test in Analog Circuits,* D.Maliuk, H.Stratigopoulos, Y.Makris (Yale U, TIMA Lab)

4.2 *Built-In Performance Monitoring of Mixed-Signal/RF Front Ends Using Real-Time Parameter Estimation*, S.Kumar Devarakond, S.Sen, A.Banerjee, V.Natarajan, A.Chatterjee (Georgia Tech)

4.3 *Wavelet Analysis of Measurements for On-Line Testing Analog and Mixed-Signal Circuits*, M.Dimopoulos, A.Spyronasios, A.Hatzopoulos (Techn. Educational Inst. of Thessaloniki, Aristotle U. of Thessaloniki)

**16:15 – 16:30: Coffee Break**

**16:30 – 17:30: Session 5 – System-Level Dependability**

Moderators: D.Pradhan (U. Bristol) and A.Bougerol (EADS)

5.1 *A Framework to Support the Design of COTS-based Reliable Space Computers for On-board Data Handling*, S.Campagna, M.Violante (Politecnico di Torino)

5.2 *Checkpointing Virtual Machines Against Transient Errors*, L.Wang, Z.Kalbarczyk, R.Iyer, A.Iyengar (University of Illinois at Urbana Champaign and IBM T.J.Watson Research Center)

5.3 *Qualification and Relifing Testing for Space Applications Applied to the Agilent G-Link Components*, M.Pignol, F.Malou, C.Aicardi (CNES)

**17:30 – 17:45: Break**

**17:45 – 18:15: Invited Talk**

*Computing with Stochastic Processors: Revisiting the Correctness Contract Between Software and Hardware*,
Rakesh Kumar (U. Illinois at Urbana-Champaign)

**18:15 – 18:30: Break**

**18:30 – 19:30: Special Session 1 – Panel: SER standards: Where we are? What's next?**

Organizers/Moderators: E.Ibe (Hitachi), M.Nicolaidis (TIMA Lab)

Panelists:

D.Alexandrescu (iRoC), R.Baumann (TI), A.Bougerol (EADS),
E.Ibe (Hitachi), S.Rezgui (Actel), C.Slayman (Ops A La Carte)

**20:00: Welcome Reception**

## Tuesday July 6, 2010

**09:00 – 10:00: Session 6 – Fault Tolerance in 3D ICs and FPGAs**

Moderators: C.Lopez-Ongil (U. Carlos III de Madrid) and F.Monteiro (U. Metz)

6.1 *Configurable Serial Fault-Tolerant Link for Communication in 3D Integrated Systems*, V.Pasca, L.Anghel, C.Rusu, M.Benabdenbi (TIMA Lab)

6.2 *RILM: Reconfigurable Inter-Layer Routing Mechanism for 3D Multi-Layer Networks-on-Chip*, C.Rusu, L.Anghel, D.Avresky (TIMA Lab, IRIANC)

6.3 *An FPGA-based Fail-soft System with Adaptive Reconfiguration*, R.Noji, S.Fujie, Y.Yoshikawa, H.Ichihara, T.Inoue (Hiroshima City U. and Hitachi)

**10:00 – 10:15: Break**

**10:15 – 11:15: Special Session 2 – On-line Monitoring for Analog and Sensor-based Systems**

Organizers/Moderators: H.Stratigopoulos (TIMA Lab) and Y.Makris (Yale U.)

S2.1 *Thermal Coupling in ICs: Applications to the Test and Characterization of Analogue Circuits*, J.Altet, D.Mateo, E.Aldrete-Vidrio, U. Politècnica de Catalunya

S2.2 *Radiation Effects on Programmable Analog Devices and Mitigation Techniques*, T.Balen, M.Lubaszewski, U. Federal do Rio Grande do Sul
S2.3 *Concepts for Fault Tolerant Sensor Systems*, A.Richardson, Lancaster U.

**11:15 – 11:30: Coffee Break**

**11:30 – 12:50: Session 7 – Memory Test, Repair, and Fault Tolerance**

Moderators: L.Dilillo (LIRMM) and V.Singh (Indian Institute of Science)

7.1 *Cross-BIC Architecture for Single and Multiple SEU Detection Enhancement in SRAM Memories*, S.A.Bota, G.Torrens, B.Alorda, J.Verd, J.Segura (U. Illes Balears)
7.2 *Programmable Restricted SEC Codes to Mask Permanent Faults in Semiconductor Memories*, S.Evain, Y.Bonhomme, V.Gherman (CEA LIST)
7.3 *A Bit Level Area Aware Cache-Based Architecture for Memory Repairs*, N.Axelos, K.Pekmestzi (National Technical U. Athens)
7.4 *A Software-Based Self-Test Methodology for In-System Testing of Processor Cache Tag Arrays*, G.Theodorou, N.Kranitis, A.Paschalis, D.Gizopoulos (U. Athens and U. Piraeus)

**12:50 – 14:00: Lunch**

**14:00 – 15:00: Session 8 – On-Line Testing Techniques**

Moderators: S.Mitra (Stanford U.) and F.Azais (LIRMM)

8.1 *An On-line Fault Detection Technique based on Embedded Debug Features*, M.Grosso, M.Sonza Reorda, M.Portela-Garcia, M.Garcia Valderas, C.Lopez-Ongil, L.Entrena (Politecnico di Torino and U. Carlos III de Madrid)
8.2 *A Partitioning Approach to Improve Reconfigurable Neuron-inspired Online BIST*, A.Shahabi, S.Behdad Hosseini, H.Sohofi, Z.Navabi (U. Tehran)
8.3 *Selecting State Variables for Improved On-Line Testability Through Output Response Comparison of Identical Circuits*, I.Pomeranz (Purdue U.), S.M.Reddy (U. Iowa)

**15:00 – 16:00: Session 9 – Posters**

9.1 *A Method for Detecting Resistive Opens in Buses*, J.Rius (UPC)
9.2 *A New Framework for the Automatic Insertion of Mitigation Structures in Circuits Netlists*, N.Battezzati, D.Serrone, M.Violante (Politecnico di Torino)
9.3 *Application Dependent FPGA Testing Method using Compressed Deterministic Test Vectors*, M.Rozkovec, J.Jenicek, O.Novak (Technical U. Liberec)
9.4 *Fully Distributed Initialization Procedure for a 2D-Mesh NoC, Including Off Line BIST and Partial Deactivation of Faulty Components*, Z.Zhang, A.Greiner, M.Benabdenbi (U. Pierre et Marie Curie & LIP6-SoC, TIMA Lab)
9.5 *Improving Fault Handling Software Techniques*, P.Gawkowski, T.Rutkowski, J.Sosnowski (Warsaw U. Technology)
9.6 *Investigating the Use of BICS to Detect Resistive-Open Defects in SRAMs*, R.Chipana, L.Veiras Bolzani, F.Vargas, J.Semiao, J.Rodriguez-Andina, I.Teixeira, J.P.Teixeira (Catholic University – PUCRS, U. Algarve, U. Vigo, IST/INESC)
9.7 *Self-Checking Arithmetic Logic Unit with Duplicated Outputs*, V.Ocheretny (Fraunhofer SIT)
9.8 *Online fault testing of reversible logic using dual rail coding*, N.Farazmand, M.Zamani, M.Tahoori (Northeastern U. and Karlsruhe Institute of Technology)
9.9 *Reconfigurable Low-Power Concurrent Error Detection in Logic Circuits*, S.Almukhaizim, S.Bunian, O.Sinanoglu (Kuwait U. and New York U. – Abu Dhabi)
9.10 *Robust Cryptographic Ciphers with On-line Statistical Properties Validation*, A.Vaskova, C.Lopez-Ongil, A.Jimenez-Horas, E.San Millan, L.Entrena (U. Carlos III of Madrid)
9.11 *Trustworthy Computing in a Multi-Core System Using Distributed Scheduling*, D.McIntyre, F.Wolff, C.Papachristou, S.Bhunia (Cleveland State U. and Case Western Reserve U.)

**16:30: Social Event (Tour and Gala Dinner)**

## Wednesday July 7, 2010

**09:00 – 09:45: Keynote Talk II**

*Statistical Design of Digital Circuits: the First Ten Years*,
Michael Orshansky (U. Texas at Austin)

**09:45 – 10:00: Break**

**10:00 – 11:00: Special Session 3 – Reliability and Test in 3D ICs**

Organizer: R.Aitken (ARM)
Moderators: K.Roy (Purdue U.) and T.Yoneda (NAIST)
S3.1 *3D Integration: Circuit Design, Test, and Reliability Challenges*, N.Minas, I.De Wolf, E.J.Marinissen, M.Stucchi, H.Oprins, A.Mercha, G.Van der Plaas, D.Velenis, P.Marchal (IMEC)
S3.2 *Interconnect Built-In Self-Repair and Adaptive-Serialization (I-BIRAS) for 3D Integrated Systems*, M.Nicolaidis, V.Pasca, L.Anghel (TIMA Laboratory)
S3.3 *Test and Reliability Concerns for 3D-ICs*, Y.Zorian (ViragеLogic)

**11:00 – 11:15: Coffee Break**

**11:15 – 12:35: Session 10 – Secure Systems**

Moderators: C.Papachristou (Case Western Reserve U.) and A.Dandache (U. Metz)
10.1 *Evaluation of Concurrent error detection techniques on the Advanced Encryption Standard*, K.Bousselam, G.Di Natale, M.-L.Flottes, B.Rouzeyre (LIRMM)
10.2 *Key Randomization using a Power Analysis Resistant Deterministic Random Bit Generator*, P.Duplys, E.Boehl, W.Rosenstiel (Robert Bosch GmbH and U. Tubingen)
10.3 *How to Flip a Bit?*, M.Agoyan, J.-M.Dutertre, A.-P.Mirbaha, D.Naccache, A.-L.Ribotta, A.Tria (CEA-LETI, EMSE, Ecole Normale Supérieure)
10.4 *Robust FSMs for Cryptographic Devices Resilient to Strong Fault Injection Attacks*, Z.Wang, M.Karpovsky (Boston U.)

**12:35 – 13:30: Lunch**

**13:30 – 14:50: Session 11 – On-Line Error Detection and Fault Tolerance**

Moderators: Y.Tsiatouhas (U. Ioannina) and M.Tahoori (Karlsruhe Inst. of Technology)
11.1 *On-Line Detection of Random Voltage Perturbations In Buses With Multiple-Threshold Receivers*, M.Skoufis (Raytheon), S.Tragoudas (Southern Illinois U.)
11.2 *Design of Embedded Constant Weight Code Checkers Based on Averaging Operations*, S.Tarnick (FBE-ASIC GmbH)
11.3 *On-line Testing of Bundled-Data Asynchronous Handshake Protocols*, S.Zeidler, A.Bystrov, M.Krstic, R.Kraemer (IHP GmbH and U. Newcastle Upon Tyne)
11.4 *Reducing the Area Overhead of TMR-systems by Protecting Specific Signals*, M.Augustin, M.Goessel, R.Kraemer (BTU Cottbus, U. Potsdam, and IHP GmbH)

**14:50 – 15:00: Break**

**15:00 – 16:00: Session 12 – Soft and Timing Error Tolerance**

Moderators: J.Rius (UPC) and I.Levin (Tel Aviv U.)
12.1 *Robust Detection of Soft Errors Using Delayed Capture Methodology*, P.V, V.Singh, R.Parekhji (Indian Institute of Science and Texas Instruments India)
12.2 *Timing Error Tolerance in Nanometer ICs*, S.Valadimas, Y.Tsiatouhas, A.Arapoyanni (U. Athens and U. Ioannina)
12.3 *Error Resilient Video Encoding Using Block-Frame Checksums*, J.Wells, J.Natarajan, A.Chatterjee (Georgia Tech.)

**16:00 – 16:15: Symposium Closing Remarks**

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