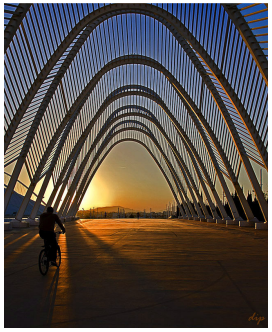

IOLTS 2011

17th IEEE
International On-Line Testing Symposium

Metropolitan Hotel, Athens, Greece

July 13-15, 2011

http://tima.imag.fr/conferences/iolts

Technical Program

Issues related to on-line testing are increasingly important in modern electronic systems. The huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective on-line testing techniques to increase the system dependability and reliability. These needs have increased dramatically with the introduction of very deep submicron and nanometer technologies which adversely impact noise margins, process, voltage and temperature variations, aging and wearout and make integrating on-line testing and fault tolerance mandatory in the majority of modern integrated circuits.

The International On-Line Testing Symposium (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The symposium also emphasizes on-line testing in the continuous operation of large applications such as wired, cellular and satellite telecommunication, as well as in secure chips. The Symposium is sponsored by the IEEE Computer Society Test Technology Technical Council and organized by the University of Athens and the TIMA Laboratory.

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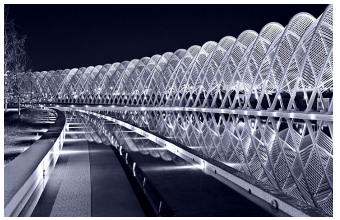
The location
Athens is the capital of Greece and is one of the world's oldest cities, as its recorded history spans around 3,400 years. Athens has been continuously inhabited for at least 7000 years. By 1400 BC the settlement had become an important center of the Mycenaean civilization and the Acropolis was the site of a major Mycenaean fortress whose remains can be recognised from sections of the characteristic Cyclopean walls. Unlike other Mycenaean centers, such as Mycenae and Pylos, it is not known whether Athens suffered destruction in about 1200 BC, an event often attributed to a Dorian invasion, and the Athenians always maintained that they were "pure" Ionians with no Dorian element. However, Athens, like many other Bronze Age settlements, went into economic decline for around 150 years following this.

The heritage of the classical era is still evident in the city, represented by a number of ancient monuments and works of art. The most famous of all being the Parthenon, widely considered a key landmark of early Western civilization. The Parthenon is a temple in the Athenian Acropolis dedicated to the Greek goddess Athena, whom the people of Athens considered their protector. Its construction began in 447 BC and was completed in 438 BC, although decorations of the Parthenon continued until 432 BC. It is the most important surviving building of Classical Greece, generally considered to be the culmination of the development of the Doric order. Landmarks of the modern era, dating back to the establishment of Athens as the capital of the independent Greek state in 1833, are located in the city center. The Hellenic Parliament (19th century) and the Athens Trilogy consisting of the National Library of Greece, the Athens University and the Academy of Athens are such landmarks.



The venue
IOLTS 2011 will be held in the Metropolitan Hotel in Athens, which uniquely combines traditional hospitality and luxury in central Athens. With a view to both the Acropolis and the Aegean Sea, the fully renovated Metropolitan hotel is ideally situated in front of the Faleron Olympic Coastal Park for both leisure and business travellers. The Metropolitan Hotel offers contemporary amenities in a relaxed and friendly atmosphere combined with traditional hospitality and impeccable service.

Social Program
The social program includes a journey back to the classical era: visit to the Acropolis, the New Museum of Acropolis, and Ancient Greek Tastes. The Acropolis of the fifth century BC is the most accurate reflection of the splendor, power and wealth of Athens at its greatest peak, the golden age of Perikles. The most important buildings visible on the Acropolis today are: the Parthenon, the Propylaia, the Erechtheion and the temple of Athena Nike. The Acropolis Museum is an archaeological museum focused on the findings of the archaeological site of the Acropolis of Athens. The collections of the museum are exhibited on three levels. On the first level of the museum there are the findings of the slopes of the Acropolis. Then, the visitor is found at the large trapezoidal hall which accommodates the archaic findings. On the same floor there are also the artifacts and sculptures from the other Acropolis buildings such as the Erechtheum, the Temple of Athena Nike and the Propylaea and findings from Roman and early Christian Athens. However the visitor is intended to see the latter during descent so as to keep the chronological order because he will first be directed to the last level of Parthenon marbles. The Parthenon hall has the same orientation with the temple on the Acropolis and the use of glass allows the natural light to enter. Our journey will be completed with dinner and thematic events at the unique thematic restaurant “Ancient Greek Tastes” (“Archeon Gefsis” in Greek). The ancient Greeks were not only eating, but they had elevated food into sheer pleasure. The cuisine is healthy, delicious and incomparable! The tastes are remarkable and forgotten! The combinations are distinctive, fine and innovative! Innovative in the sense that ancient Greeks did not have for instance potatoes, rice, tomatoes, coffee or sugar and they would use other ingredients such as honey, bulgur, legumes, thickly ground barley, surely healthier than the ones we use today.

10.16 Variations of Fault Manifestation during Burn-In - A Case Study on Industrial SRAM Test Results, M.Linder (U of Applied Sciences Augsburg), A.Eder (U of Applied Sciences Augsburg), K.Oberländer (Infineon), M.Huch (Infineon)

16:00: Social Event (Tour and Dinner)

Friday July 15, 2011

09:00 – 10:00: Session 11 – Security

Moderators: C.Papachristou (Case Western Reserve U) and C.Lopez-Ongil (U Carlos III Madrid)

11.1 A Side Channel Attack Countermeasure using System-On-Chip Power Profile Scrambling, A.Krieg, J.Grinschgl, C.Steger, R.Weiss (Graz U of Technology), J.Haid (Infineon)

11.2 AKARI-X: a Pseudorandom Number Generator for Secure Lightweight Systems, H.Martin, E.San Millan, L.Entrena (U Carlos III of Madrid), P.Peris Lopez (TU Delft), J.C.H.Castro (U Portsmouth)

11.3 Algebraic Manipulation Detection Codes and Their Applications for Design of Secure Cryptographic Devices, Z.Wang, M.Karpovsky (Boston U)

10:00 – 10:15: Break

10:15 – 11:15: Special Session 3 – Safety Critical Systems: Reliability and Survivability

Organizers: J.Abella (Barcelona Supercomputing Center), D.Gizopoulos (U Athens)

Moderator: J.Abella (Barcelona Supercomputing Center)

S3.1 Mission-critical and safety-critical systems: the challenges of the reliability and the survivability from an industrial perspective, A.Grasset, S.Yehia, P.Bonnot (Thales)

S3.2 A Cost-effective Migration from Fault Detection to Fault Tolerance in Safety-Critical Systems, R.Mariani (Yogitech)

S3.3 Industrial Requirements for Timing Analysis of Real-Time Embedded Systems, G.Bernat (Rapita Systems)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 12 – Dependability Evaluation

Moderators: D.Pradhan (Bristol U) and L.Miclea (TU of Cluj-Napoca)

12.1 A Robust Algorithm for Pessimistic Analysis of Logic Masking Effects in Combinational Circuits, T.Takata, Y.Matsunaga (Kyushu U)

12.2 An Analytical Model for the Calculation of the Expected Miss Ratio in Faulty Caches, D.Sanchez (U Murcia), Y.Sazeides (U Cyprus), J.Aragon (U Murcia), J.M.Garcia (U Murcia)

12.3 Evaluation Techniques for On-line Testing of Robust Systems Based on Critical Tasks Distribution, A.Vaskova, C.Lopez-Ongil, M.Garcia Valderas, M.Portela-Garcia, L.Entrena (Carlos III U of Madrid)

12:30 – 13:30: Lunch

13:30 – 14:30: Session 13 – Errors in DRAMs, Microprocessors, and SoCs

Moderators: I.Levin (Tel Aviv U) and N.Kranitis (U Athens)

13.1 Unidirectional Error Detection, Localization and Correction for DRAMs: Application to On-Line DRAM Repair Strategies, M.Neagu (TU of Cluj-Napoca), L.Miclea (TU of Cluj-Napoca), J.Figueras (UPC)

13.2 An Effective Methodology for On-line Testing of Embedded Microprocessors, P.Bernardi, L.Ciganda, E.Sanchez, M.Sonza Reorda (Politecnico Di Torino)

13.3 Fail-Safety in Core-Based System Design, R.Baranowski, H.-J.Wunderlich (U Stuttgart)

14:30: Symposium Closing Remarks

Wednesday July 13, 2011

07:30 – 09:00: Symposium Registration

09:00 – 10:00: Opening Session

09:00 – 09:15: Welcome Message

M.Nicolaidis (TIMA Lab), A.Paschalis (U Athens), General Chairs

D.Gizopoulos (U Athens), X.Vera (Intel Barcelona Research Center), Program Chairs

09:15 – 10:00: Keynote Talk

Reliability in the Dark Silicon Era

Prof. Babak Falsafi (EPFL)

10:00 – 10:15: Break

10:15 – 11:15: Session 1 – Degradation Modeling and Transients Tolerance

Moderators: E.Ibe (Hitachi) and A.Chatterjee (Georgia Tech)

1.1 Modeling and Mitigating NBTI in Nanoscaled Circuits, S.Khan, S.Hamdioui (TU Delft)

1.2 Investigation of Multi Cell Upset in Sequential Logic and Validity of Redundancy Technique, T.Uemura, T.Kato, H.Matsuyama (Fujitsu), K.Takahisa, M.Fukuda, K.Hatanaka (Osaka U)

1.3 High-Level Synthesis for Multi-Cycle Transient Fault Tolerant Datapaths, T.Inoue, H.Henmi, Y.Yoshikawa, H.Ichihara (Hiroshima City U)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 2 – Faults in Real-Time Systems

Moderators: S.Hellebrand (U Paderborn) and D.Alexandrescu (iRoC)

2.1 An Intellectual Property Core to Detect Task Schedulling-Related Faults in RTOS-Based Embedded Systems, D.Silva, L.Bolzani, F.Vargas (Catholic University - PUCRS)

2.2 RVC-Based Time-Predictable Faulty Caches for Safety-Critical Systems, J.Abella, E.Quiñones, F.Cazorla, M.Valero (Barcelona Supercomputing Center), Y.Sazeides (U Cyprus)

2.3 Towards Functional-Safe Timing-Dependable Real-Time Architectures, M.Paolieri (Barcelona Supercomputing Center), R.Mariani (Yogitech)

12:30 – 13:30: Lunch

13:30 – 14:30: Session 3 – Fault Tolerance

Moderators: T.Uemura (Fujitsu) and I.Polian (U Passau)

3.1 Matrix Control-Flow Algorithm-Based Fault Tolerance, R.Ferreira, A.Moreira, L.Carro (Universidade Federal do Rio Grande do Sul)

3.2 Selective Fault Tolerance for Finite State Machines, M.Augustin (BTU Cottbus), M.Goessel (U Potsdam), R.Kraemer (IHP)

3.3 A New IP Core for Fast Error Detection and Fault Tolerance in COTS-based Solid State Mass Memories, E.Costenaro, M.Violante (Politecnico di Torino), D.Alexandrescu (iRoC)

14:30 – 14:45: Break

14:45 – 15:45: Session 4 – Variability and Degradation Tolerance in Multicores

Moderators: L.Carro (UFRGS) and R.Canal (UPC)

4.1 Variability-aware Task Mapping Strategies for Many-core Processor Chips, F.Chaix, G.Bizot, M.Nicolaidis, N.Zergainoh (TIMA Laboratory)

4.2 On Graceful Degradation of Microprocessors in Presence of Faults via Resource Banking, R.Rodrigues, S.Kundu (U Massachusetts at Amherst)

4.3 On Graceful Degradation of Chip Multiprocessors in Presence of Faults via Flexible Pooling of Critical Execution Units, R.Rodrigues, S.Kundu (U Massachusetts at Amherst)

15:45 – 16:00: Coffee Break

16:00 – 17:00: Session 5 – Memory BIST

Moderators: I.Voyiatzis (TEI Athens) and F.Vargas (PUCRS)

5.1 A Multi-Objective Optimization for Memory BIST Sharing using a Genetic Algorithm, L.Zaourar (LIP6 Lab), Y.Kieffer (G-Scop Lab), A.Wenzel (ST)

5.2 Memory BIST with Address Programmability, A.Fradi, M.Nicolaidis, L.Anghel (TIMA Laboratory)

5.3 Generic BIST Architecture for Testing of Content Addressable Memories, H.Grigoryan, G.Harutyunyan, S.Shoukourian, V.Vardanian, Y.Zorian (Synopsys)

17:00 – 17:15: Break

17:15 – 18:15: Session 6 – Reliability Evaluation

Moderators: O.Heron (CEA) and M.Violante (Politecnico di Torino)

6.1 A Reliable Fault Classifier for Dependable Systems on SRAM-based FPGAs, C.Sandionigi, C.Bolchini (Politecnico di Milano)

6.2 An Approach to Reduce Computational Cost in Combinatorial Logic Netlist Reliability Analysis using Circuit Clustering and Conditional Probabilities, J.Torras Flaquer, J.Marc Daveau (ST Microelectronics), L.Naviner (GET/ENST-CNRS/LTCI), P.Roche (ST Microelectronics)

6.3 Estimation of Component Criticality in Early Design Steps, M.Sauer (U Freiburg), A.Czutro (U Freiburg), I.Polian (U Passau), B.Becker (U Freiburg)

18:15 – 18:30: Break

18:30 – 19:30: Special Session 1 – New Reliability Mechanisms in Memory Design for sub-22nm Technologies

Organizers: A.Rubio (UPC), X.Vera (Intel Barcelona)

Moderator: S.Hamdioui (TU Delft)

S1.1 Statistical variability in sub 16 nm bulk MOSFETs and FinFETs: From atomistic simulations to statistical compact models, B.Cheng (U Glasgow)

S1.2 Effect on memory systems of late CMOS technologies under variations, R.Canal (UPC)

S1.3 Hybrid reconfiguration mechanisms for heterogeneous sub-22nm multiprocessors, T.Ramirez, X.Vera (Intel Barcelona)

20:00: Welcome Reception

Thursday July 14, 2011

09:00 – 10:00: Session 7 – Testing and Error Tolerance for Low Power

Moderators: C.Bolchini (Politecnico di Milano) and E.Simeu (TIMA Lab)

7.1 A BIST Scheme for Testing and Repair of Multi-Mode Power Switches, Z.Zhang (Duke U), X.Kavousianos (U Ioannina), Y.Tsiatouhas (U Ioannina), K.Chakrabarty (Duke U)

7.2 Internal Model Control for a Self-Tuning Delay-Locked Loop in UWB Communication Systems, R.Alhakim (TIMA Lab), E.Simeu (TIMA Lab), K.Raoof (GIPSA-LAB)

7.3 Real Time Cross-Layer Adaptation for Minimum Energy Wireless Image Transport using Bit Error Rate Control, J.Natarajan, S.Sen, A.Chatterjee (Georgia Institute of Technology)

10:00 – 10:15: Break

10:15 – 11:15: Special Session 2 – Security Concerns in Modern Integrated Circuits

Organizer: Y.Makris (U Texas at Dallas)

Moderator: A.Veneris (U Toronto)

S2.1 The Cost of Cryptography in Hardware, I.Verbauwhede (K. U. Leuven)

S2.2 Countermeasures against Fault Attacks: the Good, the Bad, and the Ugly, P.Maistri (TIMA Laboratory)

S2.3 The Rise of Hardware Trojans, B.Sunar, (Worcester Polytechnic Institute)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 8 – Error Tolerant SRAM Designs

Moderators: G.Georgakos (Infineon) and L.Anghel (TIMA Lab)

8.1 A Novel Radiation Tolerant SRAM Design Based on Synergetic Functional Component Separation for Nanoscale CMOS, Y.Shiyanovskii, A.Rajendran, C.Papachristou (Case Western Reserve U)

8.2 Noise Margin, Critical Charge and Power-Delay Tradeoffs for SRAM Design, A Rajendran, Y.Shiyanovskii, F.Wolff, C.Papachristou (Case Western Reserve U)

8.3 Multiple-Bit-Upset and Single-Bit-Upset Resilient 8T SRAM Bitcell Layout with Divided Wordline Structure, S.Yoshimoto (Kobe U), T.Amashita (Kobe U), D.Kozuwa (Kyushu U), T.Takata (Kyushu U), M.Yoshimura (Kyushu U), Y.Matsunaga (Kyushu U), H.Yasuura (Kyushu U), H.Kawaguchi (Kobe U), M.Yoshimoto (Kobe U)

12:30 – 13:30: Lunch

13:30 – 14:30: Session 9 – Error Correction

Moderators: Y.Makris (U Texas at Dallas) and Y.Tsiatouhas (U Ioannina)

9.1 Error Correction Encoding for Multi-threshold Capture Mechanism, K.Karmarkar, S.Tragoudas (Southern Illinois U)

9.2 Reduced Overhead Soft Error Mitigation Using Error Control Coding Techniques, P.V (TI India), V.Singh (Indian Institute of Science), R.Parekhji (TI India)

9.3 Soft Error Correction in Embedded Storage Elements, M.Imhof, H.-J.Wunderlich (U Stuttgart)

14:30 – 15:30: Session 10 – Posters

10.1 A Comprehensive Soft Error Analysis Methodology for SoCs/ASICs Memory Instances, D.Alexandrescu (iRoC)

10.2 A Verification Strategy for Fault-Detection and Fault-Tolerance Circuits, G.Boschi, R.Mariani, S.Lorenzini (Yogitech)

10.3 Accelerating Secure Circuit Design with Hardware Implementation of Diehard Battery of Tests of Randomness, A.Vaskova, C.Lopez-Ongil, E.San Millan, A.Jimenez Horas, L.Entrena, (Carlos III U of Madrid)

10.4 An FPGA-Based Framework for Run-time Injection and Analysis of Soft Errors in Microprocessors, M.Sauer, V.Tomashevich, J.Mueller, M.Lewis, A.Spilla, I.Polian, B.Becker, W.Burgard (U Freiburg and U Passau)

10.5 An On-Line Memory State Validation Using Shadow Memory Cloning, M.Baklashov (Intel)

10.6 Control-Flow Error Recovery Using Commodity Multi-core Architecture Features, N.Khoshavi, H.Zarandi, M.Maghsoudloo (Amirkabir U of Technology)

10.7 Detection of Trojan HW by Using Hidden Information on the System, O.Keren (Bar Ilan U), I.Levin (Tel Aviv U), V.Sinelnikov (Bar Ilan U)

10.8 Fault Attack Resistant Deterministic Random Bit Generator usable for Key Randomization, E.Boehl, P.Duplys (Robert Bosch GmbH)

10.9 Fault-Tolerance Assessment and Enhancement in SoCWire Interface: A System-On-Chip Wire, R.Salamat, H.Zarandi (Amirkabir U of Technology)

10.10 Generalized Parity-Check Matrices for SEC-DED Codes with Fixed Parity, V.Gherman, S.Evain, N.Seymour, Y.Bonhomme (CEA-List)

10.11 ICT: Interface Software for the Characterization and Test of Mixed-Signal Power Cores, J.Esteves (IST - UTL), T.Moita (INESC-ID), C.Almeida (IST-UTL /INESC-ID), M.Santos (IST/INESC-ID)

10.12 Loopback Output Router for Reliable Network on Chip, C.Killian (LICM), C.Tanougast (LICM), F.Monteiro (U Paul Verlaine - Metz), A.Dandache (U Metz)

10.13 Multi-Level Secure JTAG Architecture, L.Pierce, S.Tragoudas (Southern Illinois U)

10.14 Self-Checking Test Circuits for Latches and Flip-Flops, R.Ribas, Y.Sun, A.Reis (U Federal do Rio Grande do Sul), A.Ivanov (U of British Columbia)

10.15 Software-based Control Flow Error Detection and Correction Using Branch Triplication, N.F.Ghalaty, M.Fazeli, H.Izadirad, S.G. Miremadi, (Sharif U of Technology)