IOLTS 2012

18th IEEE International On-Line Testing Symposium

Meliá Sitges Hotel, Sitges, Spain

June 27-29, 2012

http://tima.imag.fr/conferences/iolts

Technical Program

Issues related to on-line testing are increasingly important in modern electronic systems. The huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective on-line testing techniques to increase the system dependability and reliability. These needs have increased dramatically with the introduction of very deep submicron and nanometer technologies which adversely impact noise margins, process, voltage and temperature variations, aging and wearout and make integrating on-line testing and fault tolerance mandatory in the majority of modern integrated circuits.

The International On-Line Testing Symposium (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The symposium also emphasizes on-line testing in the continuous operation of large applications such as wired, cellular and satellite telecommunication, as well as in secure chips. The Symposium is sponsored by the IEEE Computer Society Test Technology Technical Council and organized by the University of Athens and the TIMA Laboratory.

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IEEE Computer Society Test Technology Technical Council (TTTC)

Organized by

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Wednesday June 27, 2012

07:30 – 09:00: Symposium Registration

09:00 – 10:00: Opening Session

09:00 – 09:15: Welcome Message

M.Nicolaidis (TIMA Lab), R.Canal (UPC), General Chairs
D.Gizopoulos (U Athens), X.Vera (Intel Barcelona Research Center), Program Chairs

09:15 – 10:00: Keynote Talk

Resilient Processors for Reliability and Energy Efficiency
Antonio Gonzalez (Director, Intel Labs, UPC, Barcelona)

10:00 – 10:20: Coffee Break

10:20 – 11:40: Session 1 – SEU Tolerance

Moderator: R.Velazco (TIMA)

1.1 Error Detection and Correction of Single Event Upset Tolerant Latch, Norhuzaimin Julai (School of Electrical,Electronic and Computer), Alexandre V Yakovlev (University of Newcastle upon Tyne), Alexander Bystrov (University of Newcastle Upon Tyne)
1.2 SETTOFF: A Fault Tolerant Flip-Flop for Building Cost-efficient Reliable Systems, Yang Lin (University of Southampton), Mark Zwolinski (Univ. of Southampton)
1.3 SEU Tolerant Robust Memory Cell Design, Shayan Mohammed (Indian Institute of Science), Virendra Singh (Indian Institute of Science (IISc)), Adit Singh (Auburn University), Fujita Masahiro (university of tokyo)
1.4 Soft Errors Resilient Logic Optimization for Low Power, Sujan Pandey, Klaas Brink (NXP Semiconductors)

11:40 – 12:00: Coffee Break

12:00 – 13:00: Session 2 – Reconfigurable Logic

Moderator: I.Koren (U Mass Amherst)

2.1 SEU-X: a SEu Un-eXcitability prover for SRAM-FPGAs, Cinzia Bernardeschi (Department of Information Engineering, University of Pisa), Luca Cassano (Department of Information Engineering, University of Pisa), Andrea Domenici (Department of Information Engineering, University of Pisa)
2.2 Analyzing and Alleviating the Impact of Errors on an SRAM-based FPGA Cluster, Arwa Ben Dhia (Telecom ParisTech), Lirida Naviner (Institut Telecom, Telecom ParisTech, CNRS LTCI), Philippe Matherat (Telecom ParisTech)
2.3 Transparent Structural Online Test for Reconfigurable Systems, Mohamed Abdelfattah (University of Stuttgart), Lars Bauer (Karlsruhe Institute of Technology), Claus Braun (University of Stuttgart), Michael Imhof (University of Stuttgart), Michael Kochte (University of Stuttgart), Hongyan Zhang (Karlsruhe Institute of Technology), Joerg Henkel (University of Karlsruhe), Hans-Joachim Wunderlich (University of Stuttgart)

13:00 – 14:00: Lunch

14:00 – 14:45: Special Session 1 – Embedded Tutorial: Online Security Monitoring for ICs

Miron Abramovici (Tiger's Lair)

14:45 – 15:00: Coffee Break

15:00 – 16:00: Session 3 – Radiation Experiments and Analysis

Moderator: O.Heron (CEA List)

3.1 A Real-Case Application of a Synergetic Design-Flow-Oriented SER Analysis, Miguel Vilchis (LSI Corporation), Ramnath Venkatraman (LSI Corporation), Enrico Costenaro (iRoC Technologies), Dan Alexandrescu (iRoC Technologies)
3.2 Fault-Based Reliable Design-On-Upper-Bound of Electronic Systems for Terrestrial Radiation Including Muons, Electrons, Protons and Low Energy Neutrons, Eishi Ibe (Hitachi, Ltd.), Tadanobu Toba (Hitachi, Ltd.), Ken-ichi Shimbo (Hitachi, Ltd.), Hitoshi Taniguchi (Hitachi, Ltd.)
3.3 Neutrons Radiation Test of Graphic Processing Units, Paolo Rech (UFRGS), Caroline Aguiar (UFRGS), Ronaldo Ferreira (Universidade Federal do Rio Grande do Sul), Christopher Frost (ISIS), Luigi Carro (Universidade Federal do Rio Grande do Sul)

16:00 – 16:20: Coffee Break

16:20 – 17:20: Session 4 – Circuit Degradation

Moderator: J.Figueras (UPC)

4.1 The Influence of Clock-Gating On NBTI-Induced Delay Degradation, Jackson Pachito (University of Algarve), Celestino Martins (University of Algarve), Jorge Semiao (Instituto Superior Engenharia - Universidade do Algarve), Marcelino Bicho Dos Santos (IST/INESC-ID), Isabel Teixeira (INESC-id), Joao Paulo Teixeira (IST, Lisboa Technical University)
4.2 Relation between HCI-induced performance degradation and applications in a RISC processor, Clement Bertolini (CEA Saclay Nano-Innov), Olivier Heron (CEA LIST), Nicolas Ventroux (CEA LIST), François Marc (Université de Bordeaux 1)
4.3 Do More Camera Pixels Result in a Better Picture?, Glenn Chapman (Simon Fraser U.), Israel Koren (University of Massachusetts), Zahava Koren (University of Massachusetts at Amherst)

17:20 – 17:50: Coffee Break

17:50 – 19:15: Special Session 2 – Panel: Cross Layer Reliability - Challenges and Standards Requirements

Organizers/Moderators: Michael Nicolaidis (TIMA), Shi-Jie Wen (Cisco)
Panelists: Magdy Abadir (Freescale), Dan Alexandrescu (iRoC), Adrian Evans (Cisco), Eishi Ibe (Hitachi), Gabriele Saucier (Design & Reuse), Yervant Zorian (Synopsys)

20:00: Welcome Reception

Thursday June 28, 2012

09:00 – 10:00: Session 5 – Memories and 3D Integration

Moderator: S.Hamdioui (TU Delft)

5.1 Low Power embedded DRAM Caches using BCH code Partitioning, Pedro Reviriego (Universidad Antonio de Nebrija), Alfonso Sancez-Macian (Universidad Nebrija), Juan Maestro (Universidad Nebrija)
5.2 On the functional test of L2 caches, Michele Riga (Politecnico di Torino), Ernesto Sanchez (Politecnico di Torino), Matteo Sonza Reorda (Politecnico Di Torino)
5.3 Through-Silicon-Via Built-In Self-Repair for Aggressive 3D Integration, Michael Nicolaidis (TIMA Laboratory), Vladimir Pasca (TIMA Laboratory), Lorena Anghel (TIMA Laboratory)

10:00 – 10:20: Coffee Break

10:20 – 11:20: Special Session 3 – Variability and Bugs: How to find them?

Organizer: P.Gupta (UCLA)
Moderator: J.Abella (BSC)

S3.1 Measuring and Monitoring Variability, P.Gupta (UCLA)
S3.2 Correlating Models and Silicon in the Presence of Variability, V.Chandra (ARM)
S3.3 Effective Post-Silicon Validation, S.Mitra (Stanford U)

11:20 – 11:40: Coffee Break

11:40 – 12:40: Session 6 – Miscellaneous

Moderator: N.Mentens (KU Leuven)

6.1 Test Access Mechanism for Chips with Spare Identical Cores, Ozgur Sinanoglu (New York University - Abu Dhabi)

6.2 RIIF - Reliability Information Interchange Format, Adrian Evans (Cisco Systems Inc.), Michael Nicolaidis (TIMA Lab), Shi-Jie Wen (Cisco) Dan Alexandrescu (iRoC Technologies), Enrico Costenaro (iRoC Technologies)

6.3 On Line Monitoring of RF Power Amplifiers with Embedded Temperature Sensors, Josep Altet (Univ Politecnica de Catalunya), Diego Mateo (DEE - UPC), Didac Gómez (DEE - UPC)

12:40 – 13:40: Lunch

13:40 – 14:40: Special Session 4 – Panel: Reliability of hard real-time systems in 32nm and beyond: who will solve the challenges?

Organizer/Moderator: S.Hamdioui (Delft U)

14:40 – 15:40: Session 7 – Posters

7.1 A Fault Attack Robust True Random Number Generator, Eberhard Boehl (Robert Bosch GmbH), Markus Ihle (Bosch)

7.2 Architectural Vulnerability Aware Checkpoint Placement in a Multicore Processor, Atieh Lotfi (University of Tehran), Arash Bayat (University of Tehran), Saeed Safari (University of Tehran)

7.3 Evaluation of Test Algorithms Stress Effect on SRAMs under Neutron Radiation, Georgios Tsiligiannis (lirmm), Luigi Dilillo (LIRMM), Alberto Bosio (LIRMM), Patrick Girard (LIRMM), Aida Todri (LIRMM), Arnaud Virazel (LIRMM), Antoine Touboul (IES/UM2), Frederic Wrobel (IES/UM2), Frédéric Saigné (IES)

7.4 Event-Driven On-Line Co-Simulation with Fault Diagnostic, Mikhail Baklashov (Intel Corporation)

7.5 Fault Coverage of a Timing and Control Flow Checker for Hard Real-Time Systems, Julian Wolf (Universitaet Augsburg), Bernhard Fechner (Universitaet Augsburg), Theo Ungerer (Universitaet Augsburg)

7.6 Fault Missing Rate Analysis of the Residue Number based Fault-Tolerant FIR Design, Zhen Gao, Wenhui Yang (Xiamen University), Xiang Chen (Tsinghua University), Ming Zhao (Tsinghua University), Jing Wang (Tsinghua University)

7.7 Functional Level Embedded Self-Testing for Walsh Transform Based Adaptive Hardware, Ariel Burg (Bar-Ilan University), Osnat Keren (Bar Ilan University)

7.8 Gatewaying IEEE 1149.1 and IEEE 1149.7 Test Access Ports, Francisco Fernandes (FEUP - Faculdade de Engenharia da Universidade do Porto), Ricardo Machado (FEUP - Faculdade de Engenharia da Universidade do Porto), Jose Ferreira (University of Porto), Manuel G. Gericota (ISEP)

7.9 Neutron-Induced Soft Error Rate Estimation for SRAM Using PHITS, Shusuke Yoshimoto (Kobe university), Takuro Amashita (Kobe University), Masayoshi Yoshimura (Kyushu Univeristy), Yusuke Matsunaga (Kyushu University), Hiroto Yasuura (Kyushu University), Shintaro Izumi (Kobe University), Hiroshi Kawaguchi (Kobe University), Masahiko Yoshimoto (Kobe University)

7.10 Pilot Symbol Driven Monitoring of Electrical Degradation in RF Transmitter Systems Using Model Anomaly Diagnosis, Sabyasachi Deyati (Georgia Institute of Technology), Aritra Banerjee (Georgia Tech), Abhijit Chatterjee (Georgia Institute of Technology)

7.11 Reliable and Secure Memories Based on Algebraic Manipulation Detection Codes, Zhen Wang (College of Eng. Boston University), Mark G. Karpovsky (College of Eng. Boston University)

16:00: Social Event (Tour and Dinner)

Friday June 29, 2012

09:00 – 10:00: Session 8 – Secure Hardware

Moderator: G.Di Natale (LIRMM)

8.1 Cross-level Protection of Circuits Against Faults and Malicious Attacks, Victor Tomashevich (U Passau), Sudarshan Srinivasan (UMass Amherst), Fabian Foerg (U Passau), Ilia Polian (University of Passau)

8.2 Punctuated Karpovsky-Taubin Binary Robust Error Detecting Codes for Cryptographic Devices, Yaara Neumeier (Bar-Ilan University), Osnat Keren (Bar Ilan University)

8.3 Stream Cipher Hash based Execution Monitoring (SCHEM) Framework for Intrusion Detection on Embedded Processors, Ameya Chaudhari (University of Texas), Jacob Abraham (University of Texas)

10:00 – 10:20: Coffee Break

10:20 – 11:20: Special Session 5 – Future Reliability Solutions: New Applications and New Devices

Organizer: D.Gizopoulos (U Athens)

Moderator: A.Chatterjee (Georgia Tech.)

S5.1 Algorithmic Techniques for Robust Applications, Rakesh Kumar (U Illinois, Urbana-Champaign)

S5.2 FinFET Technology for Memories: pros and cons, Ramon Canal (UPC)

11:20 – 11:40: Coffee Break

11:40 – 13:00: Session 9 – Soft Errors Analysis and Tolerance

Moderator: I.Levin (Tel Aviv U)

9.1 An Efficient Probability Framework for Error Propagation and Correlation Estimation, Liang Chen (Karlsruhe Institute of Technology), Mehdi Tahoori (Karlsruhe Institute of Technology)

9.2 Logic Masking for SET Mitigation Using Approximate Logic Circuits, Antonio Sanchez-Clemente (Universidad Carlos III), Luis Entrena (Universidad Carlos III), Mario Garcia Valderas (Universidad Carlos III de Madrid), Celia Lopez-Ongil (Universidad Carlos III de Madrid)

9.3 Towards Optimized Functional Evaluation of SEE-Induced Failures in Complex Designs, Dan Alexandrescu (iRoC Technologies), Enrico Costenaro (iRoC Technologies)

9.4 SEU Sensitivity of Robust Communication Protocols, Celia Lopez-Ongil (Universidad Carlos III de Madrid), Marta Portela-Garcia (Universidad Carlos III de Madrid), Mario Garcia Valderas (Universidad Carlos III de Madrid), Anna Vaskova (Carlos III University of Madrid), Luis Entrena (Universidad Carlos III), J.Rivas-Abalo, Alberto Martin-Ortega (National Institute of Aerospace Techniques), Javier Martinez Oter (National Institute of Aerospace Techniques), S.Rodrigez-Bustabad, Ignacio Arruego (National Institute of Aerospace Techniques)

13:00: Symposium Closing Remarks

13:30 – 14:30: Lunch

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The location
The name Sitges comes from “Sitja”, a pre-Roman word that means “deep hole or silo”. Even before the Neolithic period, the first *Sitgetans* lived in the area known as the “cave point” (past the Terramar golf course) and the La Punta Hill, where the church and Town Hall are today. Recently discovered archaeological remains show the existence of an Iberian settlement in the 4th-3rd century B.C. Modern studies confirm that there were two small populated areas in Sitges back in the 1st century: one around La Punta hill and another surrounding the Vinyet chapel. Along with Roman Olèrdola, Sitges’ port was used to trade products from the Penedès region and other places from the Roman Mediterranean.

Mother Nature has been generous Sitges and she has also granted the privilege of being located next to the Mediterranean Sea at the feet of the Garraf mountains. Culturally, the legacy is extraordinary, the art is alive and traditions are maintained with modernity. Sitges preserves important references from medieval and the ancient fishing village and offers visitors an important architectural heritage.

Walking through the streets of Sitges, one can admire the beautiful and unique architecture. There are houses from the locals that between the 18th century and the beginning of the 20th century emigrated to Cuba and Puerto Rico and came back to build their mansions. Part of this period was the offspring of Catalan Nouveau Art architects such as Antoni Gaudí. Some of these mansions/houses are now museums that can be visited such as: Cau Ferrat, el Palau Maricel, la Casa Bacardi.

The venue
IOLTS 2012 will be held in the Melià Sitges Hotel. It is a hotel with widely recognised experience in its ability to combine the business of professional congress and convention services with the pleasure of a resort experience. Located in the heart of the Aiguadolç marina in the northern corner of the charismatic town of Sitges, the hotel is surrounded by the Marina and Balmins beaches. Plus it is only a 10 minute walk from the centre of Sitges.

Social Program
The social program includes a trip to one of the most famous wineries in the region: Codorniu. They are a referent in *Cava* (Champagne) production. Their cava is sold worldwide and it is present in all celebrations of the Spanish Royal Family. The visit will guide us through all the production process from the grape to the bottle. Starting from the splendorous Nouveau Art building of architect Josep Puig i Cadafalch, we will visit the underground caves where Cava is left to age and, obviously, taste the local products at the end.

After the tour of the winery, we will go back to Sitges to one of its most famous local restaurants. In the "Taberna del Port" we will enjoy the local specialities. An unforgettable experience is guaranteed!