IOLTS 2013

19th IEEE International On-Line Testing Symposium

Minoa Palace Resort, Chania, Crete, Greece

July 8-10, 2013

http://tima.imag.fr/conferences/iolts

Technical Program

Issues related to on-line testing are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective on-line testing techniques. These needs have increased dramatically with the introduction of very deep submicron and nanometer technologies which adversely impact noise margins, process, voltage and temperature variations, aging and wear-out and make integrating on-line testing and fault tolerance mandatory in many modern ICs. The International On-Line Testing Symposium (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The symposium also emphasizes on-line testing in the continuous operation of large applications such as wired, cellular and satellite telecommunication, as well as in secure chips. The Symposium is sponsored by the IEEE Council on Electronic Design Automation (CEDA) and the 2013 edition is organized by the IEEE Computer Society Test Technology Technical Council, the University of Athens, and the TIMA Laboratory.

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Sunday July 7, 2013

18:00 – 19:00: Symposium Registration

Monday July 8, 2013

08:00 – 09:00: Symposium Registration

09:00 – 10:00: Opening Session

09:00 – 09:15: Welcome Message

M.Nicolaidis (TIMA Lab), A.Paschalis (U Athens), General Chairs
D.Gizopoulos (U Athens), D.Alexandrescu (iRoC), Program Chairs

09:15 – 10:00: Keynote Talk

One Thing is Certain: The Future is Unreliable
Rob Aitken (R&D Fellow, ARM)

10:00 – 10:20: Break

10:20 – 11:40: Session 1 – Fault Tolerance

Moderators: H.-J.Wunderlich (U Stuttgart) and M.Michael (U Cyprus)

1.1 Algorithm Transformation Methods to Reduce Software-only Fault Tolerance Techniques' Overhead, J.R.Azambuja (UFRGS), G.Brown (U. de la Rep), F.Kastensmidt (UFRGS), L.Carro (UFRGS)
1.2 Fault-Tolerant Adaptive Routing under Permanent and Temporary Failures for Many-Core Systems-on-Chip, M.Dimopoulos, Y.Gang, M.Benabdenbi, L.Anghel, N.-E.Zergainoh, M.Nicolaidis (TIMA Laboratory)
1.3 Hardening of Serial Communication Protocols for Potentially Critical Systems in Automotive Applications: LIN Bus, A.Vaskova, M.Portela-Garcia, M.Garcia-Valderas, C.Lopez-Ongil (Carlos III University of Madrid), M.Sonza Reorda (Politecnico Di Torino)
1.4 Highly-Reliable Integer Matrix Multiplication via Numerical Packing, I.Anarado (UCL), M.Ashraful Anam (UCL), D.Anastasia (UCL), F.Verdicchio (U Aberdeen), Y.Andreopoulos (UCL)

11:40 – 12:00: Coffee Break

12:00 – 13:00: Session 2 – Aging and Variability

Moderators: A.Evans (iRoC) and S.Hellebrand (U Paderborn)

2.1 Integrating Embedded Test Infrastructure in SRAM Cores to Detect Aging, W.Prates (Catholic University - PUCRS), L.Bolzani Poehls (Catholic University - PUCRS), G.Harutyunyan (Synopsys), A.Davtyan (Synopsys), F.Vargas (Catholic University - PUCRS), Yervant Zorian (Synopsys)
2.2 NBTI Aging Tolerance in Pipeline Based Designs, K.Katsarou (University of Ioannina), Y.Tsiatouhas (University of Ioannina), A.Arapoyanni (University of Athens)
2.3 Variability-Aware and Fault-tolerant Self-Adaptive applications for Many-Core chips, G.Bizot, F.Chaix, M.Nicolaidis, N.-E.Zergainoh (TIMA)

13:00 – 14:00: Lunch

14:00 – 15:00: Session 3 – Microprocessor Test and Vulnerability Analysis

Moderators: R.Canal (UPC) and X.Li (Chinese Academy of Science)

3.1 Increasing Fault Coverage during Functional Test in the Operational Phase, M.Carvalho, P.Bernardi, E.Sanchez, M.Sonza Reorda (Politecnico di Torino), O.Ballan (STMicroelectronics)
3.2 Investigating the limits of AVF analysis in the presence of multiple bit errors, M.Maniatakos (NYU-AD), M.Michael (U Cyprus), Y.Makris (UT Dallas)
3.3 Timing Vulnerability Factors of Sequential Elements in Modern Microprocessors, A.Bramnik (Intel), A.Sherban (Intel), N.Seifert (Intel)

15:00 – 15:20: Break

15:20 – 16:20: Session 4 – Silicon Debug and Diagnosis

Moderators: A.Chatterjee (Georgia Tech.) and P.Prinetto (Politecnico di Torino)

4.1 Accelerating Post Silicon Debug of Deep Electrical Faults, B.Le, D.Sengupta, A.Veneris, Z.Poulos (University of Toronto)
4.2 At-Speed BIST for Interposer Wires Supporting On-the-Spot Diagnosis, S.-Y.Huang, J.-C.Lee (National Tsing-Hua University), K.-H.Tsai (Mentor Graphics), W.-T.Cheng (Mentor Graphics)
4.3 A Failure Triage Engine Based On Error Trace Signature Extraction, Z.Poulos (University of Toronto), Y.-S.Yang (Vennsa), A.Veneris (University of Toronto)

16:20 – 16:40: Coffee Break

16:40 – 18:00: Session 5 – Error Detection

Moderators: S.Das (ARM) and A.Sherban (Intel)

5.1 A Software-based Self-Test strategy for online testing of the scan chain circuitries in embedded microprocessors, O.Ballan (STMicroelectronics), P.Bernardi, B.Yazdani, E.Sanchez (Politecnico di Torino)
5.2 Reducing DUE-FIT of Caches by Exploiting Acoustic Wave Detectors for Error Recovery, G.Upasani (UPC), X.Vera (Intel Barcelona Research Center), A.Gonzalez (Intel Barcelona Research Center and UPC)
5.3 Error Detection Encoding for Multi-threshold Capture Mechanism, K.Karmarkar, S.Tragoudas (Southern Illinois University, Carbondale)
5.4 Exploiting the debug interface to support on-line test of Control Flow Errors, B.Du, M.Sonza Reorda, L.Sterpone (Politecnico di Torino), L.Parra, M.Portela-Garcia, A.Lindoso, L.Entrena (University Carlos III de Madrid)

18:00 – 18:10: Break

18:10 – 19:30: Special Session 1 – Economics of Reliability

Organizer/Moderator: A.Evans (iRoC)
Ran Manor (Marvell)
Huifang Jiao (Huawei)
Yervant Zorian (Synopsys)
Jacob Abraham (U Texas at Austin)

19:45: Welcome Reception – Greek Night

Tuesday July 9, 2013

09:00 – 09:40: Session 6 – Hardware Security

Moderators: A.Grasset (Thales) and L.Anghel (TIMA)

6.1 A-SOFT-AES: Self-Adaptive Software-Implemented Fault-Tolerance for AES, F.Oboril, I.Sagar, M.Tahoori (Karlsruhe Institute of Technology)
6.2 Power supply glitch induced faults on FPGA: an in-depth analysis of the injection mechanism, L.Zussa, J.-M.Dutertre (ENSMSE), J.Clediere, A.Tria (CEA-LETI)

09:40 – 10:00: Break

10:00 – 11:20: Special Session 2 – Approximate Computing and Error Resilient Design

Organizers/Moderators: S.Mukhopadhyay (Georgia Tech.), K.Roy (Purdue U)

S2.1 Approximate Computing: Energy-efficient Computing with Good-enough Results, A.Raghunathan, K.Roy (Purdue U).

S2.2 Exploiting Application Resiliency for Energy-Efficient and Adequately-Reliable Operation, G.Karakonstantis, D.Atienza, A.Burg (EPFL)

S2.3 Error-resilient Logic Circuits under Dynamic Variations, K.Chae, S.Mukhopadhyay (Georgia Tech.)

S2.4 Challenges of RF and Mixed Signal Design under Process Variability, G.Panagopoulos, P.Riess, P.Baumgartner (Intel, Munich Germany)

11:20 – 11:40: Coffee Break

11:40 – 13:00: Session 7 – Analog Measurements and Monitoring

Moderators: D.Pradhan (Bristol U) and H.Stratigopoulos (TIMA)

7.1 Embedded High-Precision Frequency-Based Capacitor Measurement System, L.Welter (STMicroelectronics), P.Dreux (STMicroelectronics), J.-M.Portal (IM2NP), H.Aziza (IM2NP - Aix-Marseille University)

7.2 Real-Time Checking of Linear Control Systems Using Analog Checksums, S.Banerjee (Georgia Institute of Technology), A.Banerjee (Georgia Institute of Technology), A.Chatterjee (Georgia Institute of Technology), J.Abraham (University of Texas)

7.3 Perturbation-Immune Radiation-Hardened PLL with a Switchable DMR Structure, S.-N.Kim, A.Tsuchiya, H.Onodera (Kyoto University)

7.4 Scanning the Strength of a Test Signal to Monitor Electrode Degradation within Bio-Fluidic Microsystems, Q.Al-Gayem (University of Babylon), H.Liu (Cambridge Medical Innovations Ltd, UK), H.Khan (Lancaster University), A.Richardson (Lancaster University)

13:00 – 14:00: Lunch

14:00 – 15:20: Session 8 – SER Analysis

Moderators: E.Ibe (Hitachi) and A.Miele (Politecnico di Milano)

8.1 Hierarchical RTL-Based Combinatorial SER Estimation, A.Evans, D.Alexandrescu, E.Costenaro (iRoC), L.Chen (Karlsruhe Institute of Technology)

8.2 SRAM Soft Error Rate Evaluation Under Atmospheric Neutron Radiation and PVT variations, G.Tsiligiannis, E.Vatajelu, L.DiLillo, A.Bosio, P.Girard, S.Pravossoudovitch, A.Todri-Sanial, A.Virazel (LIRMM), F.Wrobel (IES), F.Saigne (IES)

8.3 State-Aware Single Event Analysis for Sequential Logic, D.Alexandrescu, E.Costenaro, A.Evans (iRoC)

8.4 Parity Check for m-of-n Delay Insensitive Codes, J.Pontes (CEA/LETI), N.Calazans (PUCRS), P.Vivet (CEA)

15:20 – 16:20: Session 9 – Posters & Coffee Break

9.1 A High Throughput Configurable Parallel Encoder Architecture for Quasi-Cyclic Low-Density Parity-Check Codes, A.Aldin Al Hariri, F.Monteiro, L.Sieler, A.Dandache (LCOMS, Université de Lorraine)

9.2 Error-Tolerance Evaluation and Design Techniques for Motion Estimation Computing Arrays, S.-K.Lu (FJCU)

9.3 Online Error Detection in Multiprocessor Chips: A Test Scheduling Study, M.Kaliorakis, N.Foutris (U Athens), M.Psarakis (U Piraeus), D.Gizopoulos (U Athens)

9.4 Evaluating a Low Cost Robustness Improvement in SRAM-based FPGAs, M.Ben-Jrad, R.Leveugle (TIMA Laboratory)

9.5 Video Decoder Monitoring using Non-linear Regression, B.Ekobo Akoa (TIMA), E.Simeu (TIMA), F.Lebowsky (STMicroelectronics)

9.6 A Low-cost Input Vector Monitoring Concurrent BIST Scheme, I.Voyiatzis, C.Efstathiou, C.Sgouropoulou (TEI of Athens)

9.7 Measuring the Performance Impact of Permanent Faults in Modern Microprocessor Architectures, N.Foutris, D.Gizopoulos (U Athens), J.Kalamatianos, V.Sridharan (AMD)

9.8 When processors get old: Evaluation of BTI and HCI effects on performance and reliability, C.Sandionigi, O.Heron, C.Bertolini, R.David (CEA)

16:30: Social Event (Tour and Dinner)

Wednesday July 10, 2013

09:00 – 10:00: Session 10 – FPGAs and Flash Memories

Moderators: J.Abraham (U Texas at Austin) and R.Leveugle (TIMA)

10.1 A Fully-Automated Flow for ITAR-free RAD-hard Atmel FPGAs, N.Andrikos (Politecnico di Torino), M.Violante (Politecnico di Torino), D.Merodio Codinachs (European Space Agency)

10.2 HHC: Hierarchical Hardware Checkpointing to Accelerate Fault Recovery for SRAM-based FPGAs, E.Yang, K.Huang Y.Hu, X.Li (Chinese Academy of Sciences), J.Gong, H.Liu, B.Liu (Beijing Institute of Control Engineering and Science and Technology on Space Intelligeent Control Lab)

10.3 EF^{3}S: an Evaluation Framework For Flash-based Systems, S.Dı Carlo, S.Galfano, M.Indaco, P.Prinetto (Politecnico di Torino)

10:00 – 10:20: Break

10:20 – 11:40: Special Session 3 – Online Hardware Security

Organizers/Moderators: O.Sinanoglu (NYU Abu Dhabi), Y.Makris (UT Dallas)

S3.1 A Post-Deployment IC Trust Evaluation Architecture, Y.Jin (U Central Florida), D.Maliuk (Yale U), Y.Makris (UT Dallas)

S3.2 On-line Testing for Differential Fault Attacks in Cryptographic Circuits, D.Mukhopadhyay (IIT Kharagpur)

S3.3 A Smart Test Controller for Scan Chains in Secure Circuits, J.Da Rolt, G.Di Natale, M.-L.Flottes, B.Rouzeyre (LIRMM)

S3.4 Scan Attack in Presence of Mode-Reset Countermeasure, S.S.Ali, S.M.Said, O.Sinanoglu (NYU Abu Dhabi), R.Karri (Polytechnic Institute of NYU)

S3.5 High Level Synthesis for Security and Trust, JV Rajendran, H.Zhang (Polytechnic Institute of NYU), O.Sinanoglu (NYU Abu Dhabi), R.Karri (Polytechnic Institute of NYU)

11:40 – 12:00: Coffee Break

12:00 – 13:20: Special Session 4 – GPUs Reliability

Organizers/Moderators: H.J.Wunderlich (U Stuttgart), D.Gizopoulos (U Athens)

S4.1 Increasing the robustness of CUDA Fermi GPU-based systems, S.Di Carlo, G.Gambardella, M.Indaco, I.Martella, P.Prinetto, D.Rolfo, P.Trotta (Politecnico di Torino)

S4.2 The Functional and Performance Tolerance of GPUs to Permanent Faults in Registers, S.Tselonis, V.Dimitsas, D.Gizopoulos (U Athens)

S4.3 Efficacy and Efficiency of Algorithm Based Fault-Tolerance on GPUs, H.-J.Wunderlich, C.Braun (U Stuttgart)

S4.4 Experimental Evaluation of GPUs Radiation Sensitivity and Algorithm-Based Fault Tolerance Efficiency, P.Rech, L.Carro (UFRGS)

13:20 – 14:20: Lunch

14:20 – 15:20: Session 11 – Errors in Memories

Moderators: D.Nikolos (U Patras) and L.Carro (UFRGS)

11.1 Accurate Alpha Soft Error Rate Evaluation in SRAM Memories, S.Bota, G.Torrens, I.De Paul, T.Alorda, J.Segura (U des les Illes Ballears)

11.2 A radiation tolerant and self-repair memory cell, N.Eftaxiopoulos-Sarris. G.Zervakis, K.Tsoumanis, K.Pekmestzi (National Technical University of Athens)

11.3 Transparent BIST for ECC-based Memory Repair, M.Nicolaidis, P.Papavramidou (TIMA)

15:20: Symposium Closing Remarks

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The location

Chania is the second largest city of Crete island and the capital of the Chania regional unit. It is a blessed and privileged place with a mild climate throughout year, countless beauties and all kinds of attractions. It is a place where different civilizations have flourished throughout the centuries. Wandering around the Old Town's maze-like alleys with the beautiful Venetian mansions, the fountains and the elaborate churches will help you discover well-preserved historical monuments.

Apart from the city of Chania, the entire region is also breathtaking. The sandy beaches, the mountain villages, the seaside hamlets, the pure nature, the Byzantine monasteries spread along the inland, the impressive gorges, such as the Gorge of Samaria with rare flora and fauna, all create a fantastic background to explore.

The city of Chania is divided in two parts: the Old Town and the modern city. The Old Town is considered the most beautiful urban district on Crete, especially the crumbling Venetian harbour. The central part of the old town is named Kasteli and has been inhabited since Neolithic times. It is located on a small hill right next to the seafront and has always been the ideal place for a settlement due to its secure position, its location next to the harbour and its proximity to the fertile valley in the south. The Splantzia quarter (next to the east part of Kasteli) is largely untouched and very atmospheric. The main square of the old town is the Eleftherios Venizelos Square. It is the heart of the touristic activities in the area. Next to this (on the west side) lies the Topanas district, which used to be the Christian part of the city during the Turkish occupation. The whole Topanas area is generally very picturesque, with many narrow alleys and old charming buildings. Finally, a very distinctive area of the old town is the harbour itself and generally the seafront with several historical buildings and a thriving nightlife.

The modern part of Chania is where most locals live and work. It is less traditional than the old town, but there are still areas of charming beauty or of some historical interest. The oldest district (early 18th century) of the modern city is Nea Hora (meaning "New Town") which is located beyond the west end of the old town. It is a developing area, but also a very picturesque one, with narrow old lanes leading to a small fishing harbour. During the same era the district of Halepa begun to grow to the east of the city and used to be home for the local aristocracy.

The venue

The 19th IEEE International On-Line Testing Symposium will be held in the Minoa Palace Resort & Spa, a luxury 5-star beachside hotel situated in the cosmopolitan area of Platanias, 12 km west of the city of Chania.

Social event: cruise and dinner

A relaxing evening cruise around one of the largest natural harbors in the word is an ideal way to top up your tan and see the sights. Boarding is at around 17:00 (departure from the Minoa Palace hotel lobby at 16:30) and after our departure from Souda harbor we sail past the island of Souda, where you can take pictures of the Venetian castle featured in the James Bond film “For Your Eyes Only”. On-board a welcome cocktail, refreshments and ice creams will be served. Our first stop is the fishing village Almirida. We have time to enjoy the beautiful beach with very clear water. The coast is full of natural caves made by the sea and after our first swim we continue to the “Cape of Drapano”. The cave is on the eastern edge of the bay and as we enter the cave in the boat you have the opportunity to take amazing pictures or videos and admire the scenery. We then change course to head south-west towards Marathi beach. We dock on the small pier by the beach and there is time to enjoy the beach sea. During our stay dinner will be served in a fish tavern nearby the beach. Our arrival back to the hotel by bus is at around 22.30.