Monday July 7, 2014

08:00 – 09:00 Symposium Registration

09:00 – 10:00 Opening Session

09:00 – 09:15 Welcome Message by General and Program Chairs

09:15 – 10:00 Keynote Talk

"GPU Reliability: Why it matters and what we can do about it?",
Prof. Murali Annavaram, University of Southern California

10:00 – 10:20 Break

10:20 – 11:20 Session 1 – Dependable Systems Design

Moderator: Magdy Abadir (Freescale)

1.1 Exploiting a Fast and Simple ECC for Scaling Supply Voltage in Level-1 Caches, Gulay YALCIN (Barcelona Supercomputing Center – Spain), Emrah ISLEK, Oyku Tozlu (TOBB University of Economics and Technology – Turkey), Pedro Reviriego (Universidad Antonio de Nebrija – Spain), Adrian CRISTAL (Barcelona Supercomputing Center & Spanish National Research Council – Spain), Osman UNSAL (Barcelona Supercomputing Center – Spain), Oguz ERGIN (TOBB University of Economics and Technology – Turkey)

1.2 Comparative study of defect-tolerant multiplexers for FPGAs, Arwa BEN DHIA (Telecom ParisTech - France), Mariem SLIMANI (Telecom ParisTech - France), Lirida NAVINER (Institut Telecom, Telecom ParisTech, CNRS LTCI - France)

1.3 Area-Efficient Synthesis of Fault-Secure NoC Switches, Atefe DALIRSANI (University of Stuttgart - Germany), Michael A. KOCHTE (University of Stuttgart - Germany), Hans-Joachim WUNDERLICH (Universitat Stuttgart - Germany)

11:20 – 11:40 Coffee Break

11:40 – 12:40 Session 2 – Advanced Nanometer Technologies

Moderator: Emmanuel Simeu (TIMA)

2.1 From an Analytic NBTI Device Model to Reliability Assessment of Complex Digital Circuits, Nasim POUR ARYAN (Technische Universitaet Muenchen - Germany), Alexandra LISTL (Technische Universitaet Muenchen - Germany), Leonhard HEISS (Technische Universitaet Muenchen - Germany), Cenk YILMAZ (Technische Universitaet Muenchen - Germany), Georg GEORGAKOS (Infineon Technologies - Germany), Doris SCHMITT-LANDSIEDEL (Technische Universitaet Muenchen - Germany)

2.2 Real-Time Transient Error and Induced Noise Cancellation in Linear Analog Filters Using Learning-Assisted Adaptive Analog Checksums, Alvaro GOMEZ-PAU (UPC - Spain), Suvadeep BANERJEE (Georgia Institute of Technology - United States), Abhijit CHATTERJEE (Georgia Institute of Technology - United States)

2.3 Pre-Bond Testing of Weak Defects in TSVs, Daniel ARUMI (UPC - Spain), Rosa RODRIGUEZ-MONTANES (UPC - Spain), Joan FIGUERAS (UPC - Spain)

12:40 – 13:40 Lunch

13:40 – 14:40 Session 3 – Hardware Security

Moderator: Claude Thibeault (E. Tech. Sup. Montreal)

3.1 Customized Cell Detector for Laser-Induced-Fault Detection, Feng LU (LIRMM - France), Giorgio DI NATALE (LIRMM - France), Marie-Lise FLOTTES (LIRMM - France), Bruno ROUZEYRE (LIRMM - France)
3.2 Precise Fault-Injections using Voltage and Temperature Manipulation for Differential Cryptanalysis, Raghavan KUMAR (University of Massachusetts, Amherst - United States), Philipp JOVANOVIC (University of Passau - Germany), Ilia POLIAN (University of Passau - Germany)
3.3 A Novel Hardware Logic Encryption Technique for Thwarting Illegal Overproduction and Hardware Trojans, Sophie DUPUIS (LIRMM - France), Papa Sidy BA (LIRMM - France), Giorgio DI NATALE (LIRMM - France), Marie-Lise FLOTTES (LIRMM - France), Bruno ROUZEYRE (LIRMM - France)

14:40 – 15:25 Poster Session 1 & Coffee Break

P1.1 A Hybrid Reliability Assessment Method and its Support of Sequential Logic Modelling, Samuel PAGLIARINI (University of Bristol - United Kingdom), Lirida NAVINER (Institut Telecom, Telecom ParisTech, CNRS LTCI - France), Jean-Francois NAVINER (Institut Telecom, Telecom ParisTech, CNRS LTCI - France), Dhiraj PRADHAN (University of Bristol - United Kingdom)
P1.2 Aging-aware Critical Paths in Deep Submicron, Phaninder ALLADI (Southern Illinois University - United States), Spyros TRAGOUDAS (Southern Illinois University - United States)
P1.3 Early Assessment of SEU Sensitivity through Untestable Faults Identification, Luca CASSANO (Politecnico di Milano - Italy), Hipolito GUZMAN-MIRANDA (Universidad de Sevilla - Spain), Miguel Angel AGUIRRE (Universidad de Sevilla - Spain)
P1.4 Timing for Virtual TMR in Logic Circuits, Sebastian MUELLER (BTU CS - Germany), Tobias KOAL (BTU Cottbus - Germany), Mario SCHOELZEL (BTU Cottbus - Germany), Heinrich VIERHAUS (BTU Cottbus-Senftenberg - Germany)
P1.5 Preliminary results of SEU Fault Injection on a Multicore processors in AMP mode, Vanessa VARGAS (TIMA Labs - France), Pablo RAMOS (TIMA Labs - France), Wassim MANSOUR (TIMA Labs - France), Jean-Francois MEHAUT (LIG Labs - France), Raoul VELAZCO (TIMA Laboratory - France), Nacer-Edinne ZERGAINOH (TIMA Laboratory – France)
P1.6 Novel Self-Test Methods to Reduce On-Chip Memory Requirements and Improved Test Coverage, Prakash NARAYANAN (Texas Instruments India Pvt. Ltd - India), Satish RAVICHANDRAN (Cadence Design Systems - India), Balaji RAMAYANAM (Mirafra Technologies - India)

15:25 – 16:25 Session 4 – Design for Reliability

Moderator: Paolo Prinetto (Politecnico di Torino)

4.1 A Noise-tolerant Master-slave Flip-flop, Yukiya MIURA, Yoshihiro OHKAWA (Tokyo Metropolitan Univ. - Japan)
4.2 New Approaches for Synthesis of Redundant Combinatorial Logic for Selective Fault Tolerance, Hao XIE (University of Saskatchewan - Canada), Li CHEN (University of Saskatchewan - Canada), Rui LIU (University of Saskatchewan - Canada), Adrian EVANS (iRoC Technologies - France), Dan ALEXANDRESCU (iRoC Technologies - France), Shi-Jie WEN (Cisco - United States), Rick WONG (Cisco - United States)

4.3 A Placement Strategy for Reducing the Effects of Multiple Faults in Digital Circuits, Samuel PAGLIARINI (University of Bristol - United Kingdom), Dhiraj PRADHAN (University of Bristol - United Kingdom)

16:25 – 16:45 Coffee Break

16:45 – 17:45 Session 5 – FPGA Reliability

Moderator: Sybille Hellebrand (U Paderborn)

5.1 Cost-efficient Testing of a Cluster in a Mesh SRAM-based FPGA, Saif Ur REHMAN (INP Grenoble - France), Mounir BENABDENBI (TIMA Laboratory, Grenoble INP-UJF-CNRS, Grenoble University - France), Lorena ANGHEL (TIMA Laboratory - France)

5.2 Towards Low-Cost Fault Detection Strategy of FPGA Configuration Memory in Real-Time Systems, Michael FRISCHKE (Robert Bosch GmbH - Germany), Andreas-Juergen ROHATSCHEK (Robert Bosch GmbH - Germany), Walter STECHELE (TU Muenchen - Germany)

5.3 A novel methodology to increase fault tolerance in autonomous FPGA-based systems, Stefano DI CARLO, Giulio GAMBARDELLA, Paolo PRINETTO, Daniele ROLFO, Pascal TROTTA, Alessandro VALLERO (Politecnico di Torino - Italy)

17:45 – 18:00 Break

18:00 – 19:20 Special Session 1 – Panel "What Reliability Issues Remain in Late CMOS Technologies?"

Organizers/Moderators: Dan Alexandrescu and Adrian Evans (iRoC Technologies)

20:00 – Welcome Reception

Tuesday July 8, 2014

09:00 – 10:00 Session 6 – Fault-Tolerant Systems

Moderator: Yiorgos Tsiatouhas (U Ioannina)

6.1 Improved Circuitry for Soft Error Correction in Combinational Logic in Pipelined Designs, Milos KRSTIC (IHP - Germany), Stefan WEIDLING (University of Potsdam - Germany), Vladimir PETROVIC (IHP - Germany), Michael GOSSEL (University of Potsdam - Germany)

6.2 Online Error Detection/Recovery for Dataflow Execution, Tiago ALVES (Universidade Federal do Rio de Janeiro - Brazil), Sandip KUNDU (University of Massachusetts - United States), Leandro MARZULO (Universidade do Estado do Rio de Janeiro - Brazil), Felipe FRANCA (Universidade Federal do Rio de Janeiro - Brazil)

6.3 A new solution to on-line detection of Control Flow Errors, Boyang DU (Politecnico di Torino - Italy), Matteo SONZA REORDA (Politecnico Di Torino - Italy), Luca STERPONE (Politecnico di Torino - Italy), Luis PARRA (University Carlos III de Madrid - Spain), Marta PORTELA-GARCIA (Universidad Carlos III de Madrid - Spain), Almudena LINDOSO (University Carlos III of Madrid - Spain), Luis ENTRENA (Universidad Carlos III - Spain)

10:00 – 10:20 Break

10:20 – 11:20 Special Session 2 – Dependable Reconfigurable Space Systems: Challenges, New Trends and Case Studies

Organizers/Moderators: Antonis Paschalis (U Athens), Pedro Reviriego Vasallo (U Antonio de Nebrija)

S2.1 Application of Controlled Concurrent Change in Scientific Space Instruments, H.Michalik (IDA, TU Braunschweig)

S2.2 Single Chip Reconfigurable RHBD Payload Data Processing Units, N.Kranitis (U Athens)

S2.3 Fault Injection Experiment on Reconfigurable CPLDs Included in OPTOS Picosatellite, C.López-Ongil (Carlos III U. Madrid)

11:20 – 11:40 Coffee Break

11:40 – 12:40 Session 7 – Soft Errors Tolerance

Moderator: Eishi Ibe (Hitachi)

7.1 Validation of a tool for estimating the effects of Soft-Errors on modern SRAM-based FPGAs, Marco DESOGUS (Politecnico di Torino - Italy), Luca STERPONE (Politecnico di Torino - Italy), David Merodio CODINACHS (European Space Agency - Netherlands)

7.2 Modified DEC BCH codes for parallel correction of 3-bit errors comprising a pair of adjacent errors, Christian BADACK (University of Potsdam - Germany), Thomas KERN (Infineon Technologies AG - Germany), Michael GOSSEL (University of Potsdam - Germany)

7.3 Double Node Charge Sharing SEU Tolerant Latch Design, Katerina KATSAROU (University of Ioannina - Greece), Yiorgos TSIATOUHAS (UNIVERSITY OF IOANNINA - Greece)

12:40 – 13:40 Lunch

13:40 – 14:25 Poster Session #2 & Coffee Break

P2.1 FF-DICE: An 8T Soft-Error Tolerant Cell using Independent Dual Gate SOI FinFETs, Nicholas AXELOS, Nikolaos EFTAXIOPOULOS, Georgios ZERVAKIS, Kostas TSOUMANIS, Kiamal PEKMESTZI (National Technical University of Athens - Greece)

P2.2 Effect of Ionizing Radiation on TRNGs for Safe Telecommunications: Robustness and Randomness, Honorio MARTIN (Universidad Carlos III de Madrid - Spain), Anna VASKOVA (Carlos III University of Madrid - Spain), Celia LOPEZ-ONGIL (Universidad Carlos III de Madrid - Spain), Enrique SAN MILLAN (Universidad Carlos III de Madrid - Spain), Marta PORTELA-GARCIA (Universidad Carlos III de Madrid - Spain)

P2.3 An Innovative Standard Cells Remapping Method for In-Circuit Critical Parameters Monitoring, Loic WELTER (STMicroelectronics - France), Philippe DREUX (STMicroelectronics - France), Hassen AZIZA (IM2NP - Aix-Marseille University - France), Jean Michel PORTAL (IM2NP - France)

P2.4 Fault Injection in GPGPU Cores to Validate and Debug Robust Parallel Applications, Mauricio CARVALHO (Politecnico di Torino - Italy), Davide SABENA (Politecnico di Torino - Italy), Matteo SONZA REORDA (Politecnico Di Torino - Italy), Luca STERPONE (Politecnico di Torino - Italy), Paolo RECH (UFRGS - Brazil), Luigi CARRO (UFRGS - Brazil)

P2.5 Multi-abstraction level signature generation and comparison based on radiation single event upset, Christelle HOBEIKA (Ecole de Technologie Superieure - Canada), Simon PICHETTE (E. Tech. Sup. Montreal - Canada), Marc-Andre LEONARD (E. Tech. Sup. - Canada), Claude THIBEAULT (E. Tech. Sup. Montreal - Canada), Jean-Francois BOLAND (E. Tech. Sup. - Canada), Yves AUDET (Ecole polytechnique Montreal - Canada)

P2.6 Managing SER Costs of Complex Systems through Linear Programming, Dan ALEXANDRESCU (iRoC Technologies - France), Nematollah BIDOKHTI, Andy YU(CISCO Systems - United States), Adrian EVANS (iRoC Technologies - France), Enrico COSTENARO (iRoC Technologies - France)

P2.7 Two complementary approaches for studying the effects of SEUs on HDL-based designs, Wassim MANSOUR (TIMA Labs - France), Miguel AGUIRRE (University of Sevilla - Spain), Hipolito GUZMAN-MIRANDA (University of Sevilla - Spain), J. BARRIENTOS (University of Sevilla - Spain), Raoul VELAZCO (TIMA Laboratory - France)

14:25 – 15:25 Session 8 – Dependability Evaluation

Moderator: Stefano Di Carlo (Politecnico di Torino)

8.1 Improving the Significance of Probabilistic Circuit Fault Emulations, David MAY (TU Muenchen - Germany), Walter STECHELE (TU Muenchen - Germany)

8.2 Error Masking With Approximate Logic Circuits Using Dynamic Probability Estimations, Antonio SANCHEZ-CLEMENTE (Universidad Carlos III de Madrid - Spain), Luis ENTRENA (Universidad Carlos III - Spain), Mario GARCIA-VALDERAS (UC3M - Spain)

8.3 Versatile Architecture-Level Fault Injection Framework for Early Reliability Evaluation, Nikos FOUTRIS (University of Athens - Greece), Manolis KALIORAKIS (University of Athens - Greece), Sotiris TSELONIS (University of Athens - Greece), Dimitris GIZOPOULOS (University of Athens - Greece)

16:00 Social Event

Wednesday July 9, 2014

09:00 – 10:00 Special Session 3 – Early Reliability Evaluation in the Computing Continuum

Organizers/Moderators: Dimitris Gizopoulos (U Athens), Stefano Di Carlo (Politecnico di Torino), Giorgio Di Natale (LIRMM)

S3.1 Revisiting Design Methods for Reliable Critical Embedded Systems, Philippe BONNOT (Thales, France)
S3.2 Reliability for Industrial Electronics, Trond LOEKSTAD, (ABB, Norway)
S3.3 Reliability in High Performance Computing, peanuts or hot potato?", Ramon CANAL (UPC, Spain)
S3.4 Combining Early Reliability Evaluation with functional safety requirements: a tool suite for safety design and verification, Francesco SFORZA (Yogitech, Italy)

10:00 – 10:20 Break

10:20 – 11:20 Session 9 – On-line and Off-Line Testing

Moderator: Ramon Canal (UPC)

9.1 Framework for Economical Error Recovery in Embedded Cores, Gaurang UPASANI (UPC - Spain), Xavier VERA (Intel Corporation - USA), Antonio GONZALEZ (Intel Barcelona Research Center and UPC - Spain)
9.2 Power-Aware Optimization of Software-Based Self-Test for L1 Caches in Microprocessors, Georgios THEODOROU (University of Athens - Greece), Nektarios KRANITIS (University of Athens - Greece), Antonis PASCHALIS (University of Athens - Greece), Dimitris GIZOPOULOS (University of Athens - Greece)
9.3 Flip-Flop Selection for In-Situ Slack-Time Monitoring based on the Activation Probability of Timing-Critical Paths, Sebastien SARRAZIN (CEA LIST - France), Samuel EVAIN (CEA - France), Ivan MIRO-PANADES (CEA LETI - France), Lirida NAVINER (Institut Telecom, Telecom ParisTech, CNRS LTCI - France), Valentin GHERMAN (CEA LIST - France)

11:20 – 11:40 Break

11:40 – 12:40 Special Session 4 – Solutions for the self-adaptation of communicating systems in operation

Organizers: H.-G.Stratigopoulos (TIMA), S.Bernard (LIRMM)
Moderator: S.Bernard (LIRMM)

S4.1 Self-Adaptive NFC Systems, M.Dieng, S.Bernard, M.Comte, F.Azaïs, M.Renovell, V.Kerzérho (LIRMM, CNRS-Université Montpellier II, France), P.-H.Pugliesi-Conti, T.Kervaon (NXP Semiconductors, France)
S4.2 Methodology for Self-Adaptation of Electronic Medical Devices: Application to an Intraocular Pressure Sensor, A.Deluthault, S.Bernard, V.Kerzérho, F.Soulier (LIRMM, CNRS-Université Montpellier II, France), P.Cauvet, L.Menzenge (Ophtimalia, France)
S4.3 One-shot Calibration of RF Power Amplifier using Non-intrusive Variation-Aware Sensors, M.Andraud, H.-G.Stratigopoulos, E.Simeu (TIMA Laboratory, CNRS – Université Grenoble Alpes, France)

12:40 – 13:40 Lunch

13:40 – 14:40 Session 10 – Field Diagnosis & Testing

Moderator: Regis Leveugle (TIMA)

10.1 Multivariate Outlier Modeling for Capturing Customer Returns – How Simple It Can Be, Jeff TIKKANEN (University of California, Santa Barbara - United States), Nik SUMIKAWA (Freescale Semiconductor - United States), Li-C. WANG (UC Santa Barbara - United States), Magdy ABADIR (Freescale Semiconductor, Inc. - USA)

10.2 Fault injection and fault handling: an MPSoC demonstrator using IEEE P1687, Kim PETERSEN (Ericsson - Sweden), Dimitar NIKOLOV (Lund University - Sweden), Urban INGELSSON (Semcon - Sweden), Gunnar CARLSSON (Ericsson - Sweden), Farrokh Ghani ZADEGAN, Erik LARSSON (Lund University - Sweden)

10.3 Permanent Faults on LIN Networks: On-line Testing Generation, Anna VASKOVA (Carlos III University of Madrid - Spain), Marta PORTELA-GARCIA (Universidad Carlos III de Madrid - Spain), Mario GARCIA-VALDERAS (UC3M - Spain), Celia LOPEZ-ONGIL (Universidad Carlos III de Madrid - Spain), Matteo SONZA REORDA (Politecnico Di Torino - Italy)

14:40 Symposium Closing Remarks