IOLTS 2015

21st IEEE
International On-Line Testing Symposium

Athena Pallas Village, Elia, Halkidiki, Greece

July 6-8, 2015

http://tima.imag.fr/conferences/iolts

Technical Program

Issues related to on-line testing are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective on-line testing techniques. These needs have increased dramatically with the introduction of very deep submicron and nanometer technologies which adversely impact noise margins, process, voltage and temperature variations, aging and wear-out and make integrating on-line testing and fault tolerance mandatory in many modern ICs. The International On-Line Testing Symposium (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The symposium also emphasizes on-line testing in the continuous operation of large applications such as wired, cellular and satellite telecommunication, as well as in secure chips. The Symposium is sponsored by the IEEE Council on Electronic Design Automation (CEDA) and the 2015 edition is organized by the IEEE Computer Society Test Technology Technical Council, the University of Athens, and the TIMA Laboratory.

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Sunday July 5, 2015

18:00 – 19:00: Symposium Registration

Monday July 6, 2015

08:00 – 09:00: Symposium Registration

09:00 – 10:15: Opening Session

09:00 – 09:15:

Welcome Message

M.Nicolaidis (TIMA Lab), A.Paschalis (U Athens), General Chairs
D.Gizopoulos (U Athens), D.Alexandrescu (iRoC), Program Chairs

In Memoriam: Adelio Salsano

09:15 – 10:15: Keynote Talk

Fault Tolerance meets Diagnosis, Hans-Joachim Wunderlich (U Stuttgart)

10:15 – 10:35: Break

10:35 – 11:35: Session 1 – Reliability Evaluation

Moderator: S.Hellebrand (U Paderborn)

1.1 Efficient Multilevel Formal Modeling, Analysis, and Estimation of Design Vulnerability to Soft Error, G.Bany Hamad (Ecole Polytechnique de Montreal), O.Ait Mohamed (Concordia), Y.Savaria (Ecole Polytechnique Montreal)

1.2 Bayesian Network Early Reliability Evaluation Analysis for both Permanent and Transient Faults, A.Vallero, A.Savino (Politecnico di Torino), S.Tselonis, N.Foutris, M.Kaliorakis (University of Athens), G.Politano (Politecnico di Torino), D.Gizopoulos (University of Athens), S.Di Carlo (Politecnico di Torino)

1.3 Laser Fault Injection into SRAM cells: Picosecond versus Nanosecond pulses, M.Lacruche (ENSM-SE), N.Borrel, C.Champeix (STMicroelectronics), C.Roscian (ENSMSE), A.Sarafianos (STMicroelectronics), J.-B.Rigaud, J.-M.Dutertre (ENSM-SE), E.Kussener (STMicroelectronics)

11:35 – 13:00: Session 2 – Posters & Coffee Break

2.1 A Call for Cross-Layer and Cross-Domain Reliability Analysis and Management, D.Alexandrescu, A.Evans, E.Costenaro, M.Glorieux (iRoC Technologies)

2.2 An Accurate Soft Error Propagation Analysis Technique Considering Temporal Masking Disablement, Y.Kimi, G.Matsukawa, S.Yoshida, S.Izumi, H.Kawaguchi, M.Yoshimoto (Kobe University)

2.3 A Hybrid Architecture for Consolidating Mixed Criticality Applications on Multicore Systems, M.Violante, S.Esposito, S.Avramenko (Politecnico di Torino), M.Sozzi, M.Traversone (Selex ES), M.Binello, M.Terrone (Alenia)

2.4 Fault Modeling and Testing Through Silicon Via Interconnections, V.Gerakis, A.Hatzopoulos (Aristotle University of Thessaloniki)

2.5 Identifying Aging-Aware Representative Paths in Processors, C.Sandionigi, O.Heron (CEA LIST)

2.6 On the Maximization of the Sustained Switching Activity in a Processor, R.Cantoro (Politecnico di Torino), H.Kerkhoff (University of Twente), A.Rohani (University of Twente), M.Sonza Reorda (Politecnico Di Torino)

2.7 Optimization of SEU Emulation on SRAM FPGAs Based on Sensitiveness Analysis, A.Souari, C.Thibeault (E. Tech. Sup. Montreal), Y.Blaquière (University of Quebec, Montreal), R.Velazco (TIMA Laboratory)

2.8 Power Analysis Attacks on ARX: An Application to Salsa20, B.Mazumdar, S.S.Ali, O.Sinanoglu (NYU-Abu Dhabi)

2.9 Simplification of Fully Delay Testable Combinational Circuits, A.Matrosova, E.Mitrofanov (Tomsk State University), T.Shah (Indian Institute of Technologies)

2.10 Soft Error Immune Latch under SEU Related Double-Node Charge Collection, K.Katsarou, Y.Tsiatouhas (University of Ioannina)

2.11 Towards Trojan Circuit Detection with Maximum State Transition Exploration, J.Lenox, S.Tragoudas (Southern Illinois University)

13:00 – 14:00: Lunch

14:00 – 15:00: Session 3 – Reliable Filters and Sensors

Moderator: Z.Stamenkovic (IHP)

3.1 Concurrent Error Detection in Nonlinear Digital Filters Using Checksum Linearization and Residue Prediction, S.Banerjee, M.Momtaz, A.Chatterjee (Georgia Institute of Technology)

3.2 Adaptive Healing Procedure for Lifetime Improvement in Wireless Sensor Networks, D.Tchuani Tchakonte, E.Simeu, (TIMA Laboratory), M.Tchuente (LIRIMA Laboratory)

3.3 Fault-Tolerant System for Catastrophic Faults in AMR Sensors, A.Zambrano, H.Kerkhoff (University of Twente)

15:00 – 15:20: Break

15:20 – 16:20: Session 4 – Fault Tolerant On-Chip Networks

Moderator: A.Grasset (Thales)

4.1 MUGEN: A High-Performance Fault-Tolerant Routing Algorithm for Unreliable Networks-on-Chip, A.Charif, N.-E.Zergainoh, M.Nicolaidis (TIMA Laboratory)

4.2 Timing-Resilient Network-on-Chip Architectures, A.Panteloukas, A.Psarras (Democritus University of Thrace), C.Nicopoulos (University of Cyprus), G.Dimitrakopoulos (Democritus University of Thrace)

4.3 Defect Diagnosis Algorithms for a Field Programmable Interconnect Network Embedded in a Very Large Area Integrated Circuit, G.Sion (UQAM), Y.Blaquière (University of Quebec, Montreal), Y.Savaria (Ecole Polytechnique Montreal)

16:20 – 16:50: Coffee Break

16:50 – 17:50: Session 5 – Fault Tolerance

Moderator: G.Georgakos (Infineon)

5.1 Design Space Exploration and Optimization of a Hybrid Fault-Tolerant Architecture, I.Wali, A.Virazel, A.Bosio, P.Girard (LIRMM), M.Sonza Reorda (Politecnico Di Torino)

5.2 Efficient On-Line Fault-Tolerance for the Preconditioned Conjugate Gradient Method, A.Scholl, C.Braun, M.Kochte, H.-J.Wunderlich (University of Stuttgart)

5.3 Mitigation of Fail-Stop Failures in Integer Matrix Products via Numerical Packing, I.Anarado, Y.Andreopoulos (UCL)

17:50 – 18:00: Break

18:00 – 19:30: Special Session 1 – The Future of Fault Tolerant Computing

Organizers/Moderators: D.Gizopoulos (U Athens), D.Alexandrescu (iRoC)
Speakers: J.Abraham (UT Austin), R.Iyer (UIUC), Y.Zorian (Synopsys)

20:00: Welcome Reception

Tuesday July 7, 2015

09:00 – 10:00: Session 6 – Error Tolerance and Prediction

Moderator: A.Paschalis (University of Athens)

6.1 Toward Efficient Check-Pointing and Rollback Under On-Demand SBST in Chip Multi-Processors, M.Skitsas, C.Nicopoulos, M.Michael (University of Cyprus)

6.2 Workload Characterization and Prediction: A Pathway to Reliable Multi-core Systems, M.Zaman, A.Ahmadi, Y.Makris (UT Dallas)

6.3 Failure Mitigation in Linear, Sesquilinear and Bijective Operations on Integer Data Streams via Numerical Entanglement, M.Anam, Y.Andreopoulos (UCL)

10:00 – 10:30: Break

10:30 – 11:30: Special Session 2 – Self-Awareness for Resilient System Design

Organizer/Moderator: M.Tahoori (U Karlsruhe)

S2.1 Runtime Reliability Prediction by Reusing DfT Infrastructure, M.Tahoori (U Karlsruhe)

S2.2 Self-Aware, Self-Learning Real-Time Systems: Application to Wireless Communications, Signal Processing and Control, A.Chatterjee (Georgia Tech.)

11:30 – 12:00: Coffee Break

12:00 – 13:00: Session 7 – Application-Specific Dependability

Moderator: M.Maniatakos (NYUAD)

7.1 Filtering-Based Error-Tolerability Evaluation of Image Processing Circuits, T.-Y.Hsieh, Y.-H. Peng (National Sun Yat-sen University)

7.2 A Single Chip Dependable and Adaptable Payload Data Processing Unit, N.Kranitis, A.Tsigkanos, G.Theodorou, I.Sideris, A.Paschalis (University of Athens)

7.3 Characterizing Fault Propagation in Safety-Critical Processor Designs, J.Espinosa, C.Hernandez, J.Abella (Barcelona Supercomputing Center)

13:00 – 14:00: Lunch

15:00: Social Event (Tour and Dinner)

Wednesday July 8, 2015

09:00 – 10:00: Session 8 – Secure and Reliable Design

Moderator: C.Lopez Ongil (U Carlos III de Madrid)

8.1 Experimental Validation of a Bulk Built-In Current Sensor in Detecting Laser-Induced Currents, C.Champeix, N.Borrel (STMicroelectronics), J.-M.Dutertre (ENSMSE), B.Robisson (CEA), M.Lisart, A.Sarafianos (STMicroelectronics)

8.2 OPUF: Obfuscation Logic Based Physical Unclonable Function, J.Ye, Y.Hu, X.Li (Institute of Computing Technology, Chinese Academy of Sciences)

8.3 Flip-Flop SEU Reduction through Minimization of the Temporal Vulnerability Factor (TVF), A.Evans, E.Costenaro (iRoC), A.Bramnik (Intel)

10:00 – 10:30: Break

10:30 – 11:30: Special Session 3 – DFx Techniques

Organizer/Moderator: M.Nicolaidis (TIMA Lab)

S3.1 An Effective Embedded Test & Diagnosis Solution for External Memories, G.Harutyunyan, Y.Zorian (Synopsys)

S3.2 Low Power Memory Repair for High Defect Densities, P.Papavramidou, M.Nicolaidis (TIMA Lab)

S3.3 Reliability/Yield Trade-Off in Mitigating "No Trouble Found" Field Returns, A.Haggag, N.Sumikawa, A.Shaukat (Freescale)

11:30 – 12:00: Coffee Break

12:00 – 13:00: Session 9 – Failure Prediction and Diagnosis

Moderator: E.Ibe (Hitachi)

9.1 Efficient Observation Point Selection for Aging Monitoring, C.Liu, M.Kochte, H.-J.Wunderlich (University of Stuttgart)

9.2 Mining Simulation Metrics for Failure Triage in Regression Testing, Z.Poulos, A.Veneris (University of Toronto)

9.3 Real-time On-chip Supply Voltage Sensor and Its Application to Trace-based Timing Error Localization, M.Ueno, M.Hashimoto, T.Onoye (Osaka University)

13:00 – 14:00: Lunch

14:00 – 15:00: Session 10 – Memory Reliability

Moderator: R.Canal (UPC)

10.1 BTI and Leakage Aware Dynamic Voltage Scaling for Reliable Low Power Cache Memories, D.Rossi, V.Tenentes (University of Southampton), S.Khursheed (University of Liverpool), B.Al-Hashimi (University of Southampton)

10.2 New Byte Error Correcting Codes with Simple Decoding for Reliable Cache Design, L.Bu, M.Karpovsky (Boston University), Z.Wang (MathWorks)

10.3 Low Leakage Radiation Tolerant CAM/TCAM Cell, N.Eftaxiopoulos, N.Axelos, K.Pekmestzi (NTUA)

15:00: Symposium Closing Remarks

The location

IOLTS 2015 will be held at Elia in the middle leg Sithonia of Halkidiki peninsula, where lush green forests reach right down to turquoise waters. Sithonia is home to the ancient city of Olynthus with its unique mosaics. It also has beaches that will take your breath away! The vegetation on Sithonía is dense. The forests - pine chiefly - reach down to the beaches -a real treat for the senses.

Shaped like Poseidon's trident and sticking out into the Aegean Sea, Halkidiki is a treat for visitors. It is a place where all your senses will come to life, whether on the endless expanses of sand of the fashionable, cosmopolitan beaches, or in the intimacy of the many secluded bays and coves. The region is formed of three peninsulas or "feet", each with its own unique charm, history and magic. There is Kassandra, or Pallini, scene of the Battle of the Giants in ancient mythology and one of Greece's most modern tourist resorts; Sithonia, a magical place of green forest and blue sea; and Mt. Athos, the world's only monastic state, home to twenty historic monasteries, untouched by the passing of time and a living monument to Byzantine culture, standing in the midst of untouched nature.

Halkidiki offers unique sightseeing like the ancient city of Olynthus where the rich villas that were excavated in the aristocratic suburb of the city are considered very important for the archaeological research since there was found some of the earliest floor mosaics in Greek art; and the Petralona cave which besides its importance for the natural beauty and size, is very important, as it presents anthropological and paleontological interest. In 1960, during the exploration works, the most important finding was the cranium of a primitive man who lived about 200,000 years ago, belongs to a transitional form, between Homo Erectus (the Standing Man) and Homo Sapiens (the Wise Man) and is the oldest testimony to the presence of humans in Greece. The cranium was covered with an encrustation of stalactite material. Fossilized bones and teeth of the regional fauna were also found, including cave bears, hyenas, lions, leopards, rhinos, deer and equids. The fossils, together with a number of tools made of stone or bones, used by the primitive inhabitant of the cave, are exhibited at the Paleontological Museum, located only a few steps away from the cave.

The venue

The 21st IEEE International On-Line Testing Symposium will be held in the Athena Pallas Village Resort. The Athena Pallas Village is located at “Akti Elia” in Sithonia peninsula in Halkidiki, at a beautiful serene with private beach. All the rooms are modernly furnished and equipped with bathroom, air condition, direct telephone connection, mini bar, balcony, and satellite TV. The hotel amenities include among others mini market, gift shop, 3 outdoor swimming pools, bar, restaurants, kid's club, bowling, billiard, movie theatre, internet access, mini golf, tennis court, spa, gym, rent a car, conference facilities. Onsite parking is complimentary. Its distance from the airport is approximately 97 km.

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