IOLTS 2016

22nd IEEE International Symposium on On-Line Testing and Robust System Design

Hotel Eden Roc, Sant Feliu de Guixols, Catalunya, Spain, July 4-6, 2016

http://tima.imag.fr/conferences/iolts/iolts16

Advance Technical Program

Issues related to on-line testing techniques, and more generally to design for robustness, are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective design for robustness techniques. These needs have increased dramatically with the introduction of nanometer technologies, which impact adversely noise margins; process, voltage and temperature variations; aging and wear-out; soft error and EMI sensitivity; power density and heating; and make mandatory the use of design for robustness techniques for extending yield, reliability, and lifetime of modern integrated circuits. Design for reliability becomes also mandatory for reducing power dissipation, as voltage reduction, often used to reduce power, strongly affects reliability by reducing noise margins and thus the sensitivity to soft-errors and EMI, and by increasing circuit delays and thus the severity of timing faults. There is also a strong relation between design for reliability and design for security, as security attacks are often fault-based. The International Symposium on On-Line Testing and Robust System Design (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The Symposium is sponsored by the IEEE Council on Electronic Design Automation (CEDA) and the 2016 edition is organized by the IEEE Computer Society Test Technology Technical Council, the University of Athens, and the TIMA Laboratory. IOLTS this year is held as part of the 1st Federative Event on Design for Robustness (FEDfRo – http://tima.imag.fr/conferences/fedfro/fedfro16/.)

Sponsored by
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The location

IOLTS 2016 will be held at Sant Feliu de Guixols, Costa Brava, Spain. The area offers a brilliant experience, with so much to offer: a beautiful natural setting, culture, leisure, sport, and a delightful seafront location with a multitude of idyllic small coves and longer bays with fine and golden sand. Sant Feliu de Guixols has also an impressive monumental site, formed by the parish church and different elements from the Romanesque monastery of the village, with its famous Porta Ferrada. Sant Feliu de Guixols is close to the main communication routes, in the Costa Brava area, and is situated at:

32 km from Girona Airport (33 min by car). Private door-to-door transportation between Girona Airport and Sant Feliu de Guixols: 47 €

118 km from Barcelona Airport (1 hour 23 min by car). Bus company Sarbus ensures 14 daily trips between Barcelona Airport and Sant Feliu de Guixols: 17 € cost, about 2 hours trip

108 km from Barcelona (1 hour 22 min by car)

80 km from Figueres: birthplace Salvador Dalí, housing the Dalí Theatre-Museum considered as the largest surrealistic object in the world

98 km from the French borders

281 km from Montpellier, France (2 hours 59 min by car)

The venue

The 22nd IEEE International Symposium on On-Line Testing and Robust System Design will be held at the hotel Eden Roc, located at a 1 km from Sant Feliu de Guixols, and 8 minutes walking distance from the main golden sandy beach of the town. Eden Roc is built on the seafront rocks of a unique and quiet peninsula, enjoying stunning sea views, and is situated at few meters from the seafront, with its nice terraces, gardens, and swimming pools touching the sea. Along the coast in either direction are a multitude of small coves and longer bays with fine sand and many services. You can spend your entire holiday on a different beach every day. The hotel amenities include among others, freshwater and seawater outdoor swimming pools, heated indoor swimming pool, comfortable lounges, elegant living rooms, 2 bars, own bridge and billiards room, health center, massage service, hot tubs, 2 restaurants with abundant barbecue buffet at noon and in the evening a buffet with elected specialties of the region.

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Monday July 4, 2016

08:00 – 09:00: Registration

09:00 – 10:00: FEDFRO Opening Session

09:00 – 09:15: Welcome Message

M.Nicolaidis (TIMA Lab), F.Azais (LIRMM), M.Abadir (Abadir & Assoc.)
FEDFRO Coordinators

09:15 – 10:00: FEDFRO Keynote Talk

Driving opportunities and technical challenges of the next wave of semiconductors devices, Karim Arabi (Vice President R&D Qualcomm)

10:00 – 10:15: Break

10:15 – 11:15: IOLTS Opening Session

10:15 – 10.30: Symposium Introduction

M.Nicolaidis (TIMA Lab), General Chair
D.Gizopoulos (U Athens), D.Alexandrescu (iRoC), Program Chairs

10:30 – 11:15: IOLTS Keynote Talk

Starting the journey towards resilient automotive electronics, Franz Dietz (Bosch)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 1 – Posters

1.1 On the robustness of DCT-based compression algorithms for space applications, S.Avramenko, M.Sonza Reorda, M.Violante (Politecnico di Torino), G.Fey (U Bremen / DLR), J.-G.Mess, R.Schmidt (DLR)
1.2 Analytic Models for Crossbar Read Operation, A.Adeyemo, X.Yang, A.Bala (Oxford Brookes U), J.Mathew (IIT Patna), A.Jabir (Oxford Brookes U)
1.3 A Fault-tolerant Sequential Circuit Design for SAFs and PDFs Soft Errors, A.Matrosova, S.Ostanin, I.Kirienko, E.Nikolaeva (Tomsk State U)
1.4 ACM: Accurate Crosstalk Modeling to Predict Channel Delay in Network-on-Chips, Z.Mahdavi, Z.Shirmohammadi, S.G.Miremadi (Sharif U Technology)
1.5 An On-Line Test Solution for Addressing Interconnect Shorts in on-Chip Networks, B.Bhowmik, J.K.Deka, S.Biswas (IIT Guwahati)
1.6 An Soft Error Propagation Analysis Considering Logical Masking Effect on Re-convergent Path, S.Yoshida, G.Matsulawa, S.Izumi, H.Kawaguchi, M.Yoshimoto (Kobe U)
1.7 Analysis of BTI Aging of Level Shifters, J.Cai, B.Halak, D.Rossi (U Southampton)
1.8 Cache-aware Reliability Evaluation through LLVM-based Analysis and Fault Injection, M.Kooli, G.Di Natale, A.Bosio (LIRMM)
1.9 Comparison of RTL Fault Models for the Robustness Evaluation of Aerospace FPGA devices, V.Beroulle, R.Champon, A.Papadimitriou (Grenoble Alpes U), D.Hely (Grenoble INP), G.Genevrier, F.Cezilly (Thales)
1.10 Efficient Fault-tolerant Parallel Matrix-Vector Multiplications, Z.Gao (Tianjin U), P.Reviriego, J.-A.Maestro (U Antonio de Nebrija)

12:30 – 13:45: Lunch

13:45 – 14:45: Session 2 – Robust Memories

Moderator: A.Grasset (Thales)
2.1 Resilient Random Modulo Cache Memories for Probabilistically-Analyzable Real-Time Systems, D.Trilla, C.Hernandez, J.Abella (BSC), F.J.Cazorla (BSC, IIIA-CSIC)
2.2 Statistical Analysis and Comparison of 2T and 3T1D e-DRAM Minimum Energy Operation, M.Rana, R.Canal, E.Amat, A.Rubio (UPC)
2.3 Variations-Tolerant 9T SRAM Circuit with Robust and Low Leakage SLEEP Mode, H.Jiao, Y.Qiu (Eindhoven U of Technology), V.Kursun (The Hong Kong U of Science and Technology)

14:45 – 15:00: Break

15:00 – 16:00: Special Session 1 – EDA Support for Functional Safety

Organizer/Moderator: D.Alexandrescu (iRoC)
S1.1 How EDA can Improve Productivity in the Assessment of Functional Safety, D.Alexandrescu (iRoC)
S1.2 Infrastructure IP of SOCs in Automotive Applications, Y.Zorian (Synopsys)

16:00 – 16:30: Coffee Break

16:30 – 17:30: Special Session 2 – Aging Modeling and Mitigation

Organizer/Moderator: Florian Cacho (STMicroelectronics)
S2.1 Hot-Carrier and BTI Damage Distinction for High Performance Digital Application in 28nm FDSOI and 28nm LP CMOS nodes, A.Bravaix, M.Saliva, F.Cacho, X.Federspiel, C.Ndiaye, S.Mhira, E.Kussener, E.Pauly, V.Huard (IM2NP-ISEN & STMicroelectronics)
S2.2 Activity Profiling: review of different solutions to develop reliable and performant design, F.Cacho, A.Benhassain, S.Mhira, A.Sivadasan, V.Huard, P.Cathelin, V.Knopik, A.Jain, C.Parthasarathy, L.Anghel (STMicroelectronics & TIMA)
S2.3 Fine-grain analysis of the parameters involved in aging of digital circuits, B.Ouattara, O.Heron, C.Sandionigi (CEA-LIST)

17:30 – 17:45: Break

17:45 – 18:45: Session 3 – "To Inject or not to Inject?"

Moderator: A.Paschalis (U Athens)
3.1 Evaluating Application-Aware Soft Error Effects in Digital Circuits without Fault Injections or Probabilistic Computations, K.Chibani, M.Portolan, R.Leveugle (TIMA Laboratory)
3.2 Modeling RTL Fault Models Behavior to Increase the Confidence on TSIM-based Fault Injection, J.Espinosa (UPV), C.Hernandez (BSC), J.Abella (BSC)
3.3 Revisiting Software-based Soft Error Mitigation Techniques via Accurate Error Generation and Propagation Models, M.Ebrahimi, M.Rashvand (Karlsruhe Institute of Technology), F.Kaddachi (LIRMM), M. Tahoori (Karlsruhe Institute of Technology), G.Di Natale (LIRMM)

18:45 – 19:00: Break

19:00 – 20:00: Session 4 – Validation and Verification

Moderator: S.Hellebrand (U Paderborn)
4.1 ISA-Independent Post-Silicon Validation for the Address Translation Mechanisms of Modern Microprocessors, G.Papadimitriou, A.Chatzidimitriou, D.Gizopoulos (U Athens), R.Morad (IBM Research Labs)
4.2 Flexible in-Silicon Checking of Run-Time Programmable Assertions, Y.Zhou, O.Bringmann, W.Rosenstiel (U Tuebingen)
4.3 Hardware-Simulation Correlation of Timing Error Detection Performance of Software-based Error Detection Mechanisms, Y.Masuda, M.Hashimoto, T.Onoye (Osaka U)

20:00: Welcome Reception

Tuesday July 5, 2016

09:00 – 10:00: Session 5 – Degradation

Moderator: S.Di Carlo (Politecnico di Torino)
5.1 On-line Write Margin Estimator to Monitor Performance Degradation in SRAM Cores, B.Alorda, C.Carmona, G.Torrens, S.Bota (U Illes Balears)

5.2 Recovery of Performance Degradation in Defective Branch Target Buffers, F.Filippou, G.Keramidas, M.Mavropoulos, D.Nikolos (U Patras)
5.3 NBTI Aging Evaluation of PUF-based Differential Architectures, M.S.Mispan, B.Halak, M.Zwolinski (U Southampton)

10:00 – 10:15: Break

10:15 – 11:15: Session 6 – Fault Tolerance Techniques

Moderator: M.Violante (Politecnico di Torino)

6.1 REMO: Redundant Execution with Minimum Area, Power, Performance Overhead Fault Tolerant Architecture, S.Gopalakrishnan, V.Singh (IIT Bombay)
6.2 Susceptible-Workload driven Selective Fault Tolerance using a Probabilistic Fault Model, M.Gutierrez, V.Tenentes, T.Kazmierski (U Southampton)
6.3 Temperature- and Aging-Resistant Inverter for Robust and Reliable Time to Digital Circuit Designs in a 65nm Bulk CMOS Process, K.Tscherkaschin, T.Hillebrand, M.Taddiken, S.Paul, D.Peters-Drolshagen (U Bremen)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Special Session 3 – Advanced Fault Tolerant Techniques for Reliability and Low-Power

Organizer/Moderator: M.Nicolaidis (TIMA Lab)

S3.1 Leakage mitigation for low power microcontroller design in 40nm for internet-of-things (IoT), A.Kapoor, N.Engin, J.Verdaasdonk (NXP)
S3.2 Advanced Double-Sampling Architectures, M.Nicolaidis, M.Dimopoulos (TIMA Lab)
S3.3 Pushing the Limits: How Fault Tolerance Extends the Scope of Approximate Computing, H.-J.Wunderlich, C.Braun, A.Schöll (U Stuttgart)

12:30 – 13:45: Lunch

13:45 – 14:45: Session 7 – Soft Errors Mitigation

Moderator: R.Velazco (TIMA)

7.1 Tackling Long Duration Transients in Sequential Logic, E.Koser, W.Stechele (TU Munich)
7.2 HLS-based Sensitivity-Inductive Soft Error Mitigation for Satellite Communication Systems, X.Chen (Sun Yat-sen U), W. Yang (BCIA), M.Zhao, J.WANG (Tsinghua U)
7.3 An Efficient LDPC Encoder Architecture for Space Applications, D.Theodoropoulos, A.Paschalis, N.Kranitis (U Athens)

16:00: Social Event

Wednesday July 6, 2016

09:00 – 10:00: Session 8 – Fault Detection and Diagnosis

Moderator: N.-E.Zergainoh (TIMA)

8.1 Scalable FPGA Graph model to detect routing faults, L.Sterpone, G.Cabodi, S.F.Finocchiaro, C.Loiacono, F.Savarese, B.Du (Politecnico di Torino)
8.2 Concurrent Error Detection and Tolerance in Kalman Filters Using Encoded State and Statistical Covariance Checks, S.Pandey, S.Banerjee, A.Chatterjee (Georgia Institute of Technology)
8.3 Automatic Generation of Stimuli for Fault Diagnosis in IEEE 1687 Networks, R.Cantoro, M.Montazeri, M.Sonza Reorda (Politecnico Di Torino), F.Ghani Zadegan, E.Larsson (Lund U)

10:00 – 10:15: Break

10:15 – 11:15: Session 9 – Reliability Pot-Pourri

Moderator: L.Anghel (TIMA)

9.1 RIIF-2: toward the next generation Reliability Information Interchange Format, A.Savino, S.Di Carlo, A.Vallero, G.Politano (Politecnico di Torino), D.Gizopoulos (U Athens), A.Evans (iRoC)
9.2 STT-MTJ-based TRNG with On-The-Fly Temperature/Current Variation Compensation, E.Vatajelu (Politecnico di Torino), G.Di Natale (LIRMM), P.Prinetto (Politecnico di Torino)
9.3 SET Response of a SEL Protection Switch for 130 and 250 nm CMOS Technologies, M.Andjelkovic, A.Ilic (U Nis), V.Petrovic, M.Nenadovic, Z.Stamenkovic (IHP), G.Ristic (U Nis)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 10 – Posters

10.1 Reusing Logic Masking to Facilitate Path-Delay-Based Hardware Trojan Detection, A.Nejat, D.Hely, V.Beroulle (Grenoble Alpes U)
10.2 Evaluation of machine learning algorithms for Image Quality Assessment, R.Alhakim, G.Takam Tchendjou, E.Simeu (TIMA Laboratory), F.Lebowsky (STMicroelectronics)
10.3 An Odd-Even Scheme to Prevent a Packet from Being Corrupted and Dropped in Fault Tolerant NoCs, B.Bhowmik, S.Biswas, J.K.Deka (IIT Guwahati)
10.4 Feasibility of Software-based Repair for Program Memories, P.SKONCEJ (BTU Cottbus-Senftenberg), F. Muhlbauer, F.Kubicek, L.Schroder, M.Scholzel (U of Potsdam)
10.5 Hardware Trojans Classification for Gate-level Netlists based on Machine Learning, K.Hasegawa, M.Oya, M.Yanagisawa, N.Togawa (Waseda U)
10.6 On the influence of compiler optimizations in the fault tolerance of embedded systems, A.Serrano-Cases, J.Isaza-Gonzalez, S.Cuenca-Asensi, A.Martinez-Alvarez (U Alicante)
10.7 Online Monitoring of NBTI and HCD in Beta-Multiplier Circuits, T.Hillebrand, M.Taddiken, K.Tscherkaschin, S.Paul, D.Peters-Drolshagen (U Bremen)
10.8 Online Monitoring of the Maximum Angle Error in AMR Sensors, A.Zambrano, H.Kerkhoff (U Twente)
10.9 Online Time Interference Detection in Mixed-Criticality Applications on Multicore Architectures using Performance Counters, S.Esposito, M.Violante (Politecnico di Torino), M.Sozzi, M.Terrone, M.Traversone (Finmeccanica)
10.10 Power-Side-Channel Analysis of Carbon Nanotube FET Based Design, C.K.H.Suresh, B.Mazumdar, S.S.Ali, O.Sinanoglu (New York U-Abu Dhabi)
10.11 Redesign for Untrusted Gate-level Netlists, M.Oya (Waseda U, NEC), M.Yanagisawa, N.Togawa (Waseda U)

12:30 – 13:45: Lunch

13:45 – 14:45: Session 11 – Robust Storage Elements

Moderator: A.Rubio (UPC)

11.1 Single-Event Performance of Differential Flip-Flop Designs and Hardening Implication, R.M.Chen (Tsinghua U), E.X.Zhang, B.L.Bhuva, L.W.Massengill, W.T.Holman (Vanderbilt U)
11.2 Conditional Soft-Edge Flip-Flop for SET Mitigation, P.Sismanoglou, D.Nikolos (U Patras)
11.3 A High Performance Scan Flip-Flop Design for Serial and Mixed Mode Scan Test, S.Ahlawat (IIT Bombay), J.Tudu (IIS Bangalore), A.Matrosova (Tomsk State U), V.Singh (IIT Bombay)

14:45 – 15:00: Break

15:00 – 16:00: Session 12 – Security

Moderator: E.Sanchez (Politecnico di Torino)

12.1 Binary decision diagram to design balanced secure logic styles, H.KIM (KU Leuven and iMinds), S.Hong (Korea U), B.Preneel, I.Verbauwhede (KU Leuven and iMinds)
12.2 A Hybrid Self-diagnosis Mechanism with Defective Nodes Locating and Attack Detection for Parallel Computing Systems, L.Bu, M.Karpovsky (Boston U)
12.3 Hardware Enlightening: No Where to Hide Your Hardware Trojans, M.S.Samimi, E.Aerabi, Z.Kazemi, M.Fazeli, A.Patooghy (Iran U of Science and Technology)

16:00: Symposium Closing Remarks