CALL FOR PAPERS
23rd IEEE International Symposium on
On-Line Testing and Robust System Design

Hotel Macedonia Palace, Greece, July 3-5, 2017

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Issues related to On-line testing techniques, and more generally to design for robustness, are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective design for robustness techniques. These needs have increased dramatically with the introduction of nanometer technologies, which impact adversely noise margins; process, voltage and temperature variations; aging and wear-out; soft error and EMI sensitivity; power density and heating; and make mandatory the use of design for robustness techniques for extending, yield, reliability, and lifetime of modern SoCs. Design for reliability becomes also mandatory for reducing power dissipation, as voltage reduction, often used to reduce power, strongly affects reliability by reducing noise margins and thus the sensitivity to soft-errors and EMI, and by increasing circuit delays and thus the severity of timing faults. There is also a strong relation between Design for Reliability and Design for Security, as security attacks are often fault-based.

The International Symposium on On-Line Testing and Robust System Design (IOLTS), is an established forum for presenting novel ideas and experimental data on these areas. The Symposium is sponsored by the IEEE Council on Electronic Design Automation (CEDA) and the 2017 edition is organized by the IEEE Computer Society Test Technology Technical Council, the University of Athens, and the TIMA Laboratory.

The topics of interest include (but are not limited to) the following ones:

- Quality, yield, reliability and lifespan issues in nanometer technologies
- Variability, Aging, EMI, and Radiation Effects in nanometer technologies
- Self-Test and Self-Repair
- Design-for-Reliability
- On-line testing techniques for digital, analog and mixed-signal circuits
- Self-checking circuits and coding theory
- On-line monitoring of current, temperature, process variations, and aging
- Self-Healing design
- Self-Regulating design
- Self-Adapting design
- Cross-layer reliability approaches
- Reliability issues of Low-Power Design

- Design for Reliability approaches for Low-Power
- Power density and overheating issues in nanometer technologies
- Fault-Tolerant and Fail-Safe systems
- Dependable system design
- Field Diagnosis, Maintainability, and Reconfiguration
- Design for Security
- Fault-based attacks and counter measures
- Design for Robustness for automotive, railway, avionics, space, large industrial applications, IT infrastructure, cloud computing, and wired, cellular and satellite communications
- Robustness evaluation
- CAD for robust circuits design

NEW This year IOLTS puts particular emphasis on the topics of:

Robust Automotive Electronics
- Design for Robustness is gaining importance in Automotive electronics, due to their stringent Reliability, Security, and Extended Lifespan constraints, which are strongly impacted by the rapidly increasing complexity of automotive electronics and the introduction of advanced nanometric processes

Design for Robustness versus Design for Low-Power
- Design for Security, as well as Fault Mitigation techniques used for improving Yield, Reliability, and Lifespan, may increase power dissipation. Thus, targeting low-power penalties when developing Design for Robustness approaches is becoming mandatory.
- Voltage reduction (often used to reduce power), strongly affects yield, reliability, and lifespan, by reducing noise margins and thus the sensitivity to EMI and soft-errors; an by increasing circuit delays and thus the severity of timing faults; as well as by further weakening to the point of failure cells that are weak (due to process variations and aging) but not yet failing.
- Last but not least, drastic power reduction can be achieved by means of fault mitigation approaches (like those used in Design for Reliability, Yield, and Lifespan techniques); by reducing aggressively the supply voltage and using these approaches to mitigate the failures induced by this reduction.

Submissions: The IOLTS Committee invites authors to submit papers in the above or related technical areas. Accepted papers and posters will be included in formal Proceedings to be published by the IEEE. Papers must be submitted electronically following the instructions provided at the symposium web site. Papers should be in the standard IEEE conferences double-column format. If accepted, regular papers should be allowed six pages in the IEEE proceedings of IOLTS.

Please observe the following key dates:

Submission deadline: **February 28, 2017** – Notification of acceptance: **April 6, 2017** – Camera-ready papers due: **May 7, 2017**

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Federative Event on Design for Robustness (FEDfRo): IOLTS'17 is held as part of the 2nd Federative Event on Design for Robustness (FEDfRo). For all details about the event see: http://tima.imag.fr/conferences/fedfro/fedfro17/.

About the location: IOLTS 2017 will be held at Thessaloniki, Greece. The area offers a brilliant experience, with so much to offer:
The beautiful bay of Thermaikos, its archeological sites and museums, and its cosmopolitan character

For all updated information concerning IOLTS 2017, please visit the IOLTS web site: http://tima.imag.fr/conferences/iolts

TIMA Laboratory   University of Athens