IOLTS 2018

24th IEEE International Symposium on On-Line Testing and Robust System Design

Hotel Cap Roig, Platja d'Aro, Costa Brava, Spain, July 2-4, 2018

http://tima.univ-grenoble-alpes.fr/conferences/iolts/iolts18/

Final Technical Program

Issues related to On-line testing techniques, and more generally to design for robustness, are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective design for robustness techniques. These needs have increased dramatically with the introduction of nanometer technologies, which impact adversely noise margins; process, voltage and temperature variations; aging and wear-out; soft error and EMI sensitivity; power density and heating; and make mandatory the use of design for robustness techniques for extending, yield, reliability, and lifetime of modern SoCs. Design for reliability becomes also mandatory for reducing power dissipation, as voltage reduction, often used to reduce power, strongly affects reliability by reducing noise margins and thus the sensitivity to soft-errors and EMI, and by increasing circuit delays and thus the severity of timing faults. There is also a strong relation between Design for Reliability and Design for Security, as security attacks are often fault-based. The International Symposium on On-Line Testing and Robust System Design (IOLTS), is an established forum for presenting novel ideas and experimental data on these areas. The Symposium is sponsored by the IEEE Council on Electronic Design Automation (CEDA) and the 2018 edition is organized by the IEEE Computer Society Test Technology Technical Council, the University of Athens, and the TIMA Laboratory. IOLTS 2018 is held for third year as part of the 3rd Federative Event on Design for Robustness (FEDfRo – http://tima.univ-grenoble-alpes.fr/conferences/fedfro/fedfro18/).

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The location and venue

The 24th IEEE International On-Line Testing Symposium will be held in the hotel Cap Roig, situated at Platja d'Aro. Hotel Cap Roig is built on the rocks of the Platja D'Aro coast, enjoying stunning sea views and giving access to a private beach. The elevator from the hotel lobby brings the guests to the rocky seafront, where a 90 meter wood made path, traversing the rock formations, leads to a set of small sandy beaches, starting with the sublime setting of the Cap Roig beach.

Platja d'Aro sits alongside the other two settlements of the municipality Castell-Platja d'Aro: The elegant S'Agaro, and the old town Castell d'Aro, build around a medieval castle and fortified church bursting with medieval charm. The seafront of Platja d'Aro is full of beaches and small coves, spanning from the two kilometers soft, golden sand, of the main beach, to several small corners where the water and the trees almost touch, leaving a narrow strip of sand.

Beyond the bustling seafront, and several artistic constructs there is a whole natural world to be discovered with delights like the Gavarres mountain range, and the Parc dels Estanys, a natural setting in the heart of the city, offering an educational route with several watchtowers to observe more 250 species of birds that inhabit the wetland.

At 78 Kms from Platja d'Aro the town of Figueres birthplace Salvador Dalí is situated. It houses the Dalí Theatre-Museum, designed Dali himself. Considered as the largest surrealistic object in the world, it contains the broadest range of works spanning the artistic career of Salvador Dalí, from his earliest artistic experiences — Impressionism, Futurism, Cubism, etc. — and his surrealist creations down to the works of the last years of his life.

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Monday July 2, 2018

07:30 – 08:30: Registration

08:30 – 09:30: FEDFRO Opening Session

08:30 – 08:45: Welcome Message

08:45 – 09:30: FEDFRO Keynote Talk

Emerging Discontinuities in Design and Verification Methodologies
W.Rhines (Mentor Graphics President and CEO), Moderator: M. Abadir (Helic)

09:30 – 09:45: Break

09:45 – 10:00: IOLTS Opening Session

M.Nicolaidis (TIMA Lab), A.Rubio (UPC), General Chairs
D.Gizopoulos (U Athens), D.Alexandrescu (iRoC), Program Chairs

10:00 – 11:00: Session 1 – Aging

Moderator: A.Bramnik (Intel)

1.1 Integrated Test Structures for Reliability Investigation under Dynamic Stimuli, F.Cacho, D.Nouguier, M.Arabi, X.Federspiel, Y.Carminati, M.Saliva (STMicroelectronics)
1.2 Near-Optimal Node Selection Procedure for Aging Monitor Placement, S.Sadeghi-Kohan, A.Vafaee, Z.Navabi (U Tehran)
1.3 Periodic Aging Monitoring in SRAM Sense Amplifiers, H.-M.Dounavi, Y.Sfikas, Y.Tsiatouhas (U Ioannina)

10:00 – 11:00: Session 2 – Mixed-Signal and RF Testing

Moderator: M.Andraud (KU Leuven)

2.1 Low-cost functional test of a 2.4GHz OQPSK transmitter using standard digital ATE, T.Vayssade, F.Azais, L.Latorre, F.Lefevre (NXP, LIRMM)
2.2 AMS-RF test quality: Assessing defect severity, V.Gutierrez, A.Gines, G.Leger (U Sevilla)
2.3 Reduced-code static linearity test of SAR ADCs using a built-in incremental ΣΔ converter, R.Feitoza, M.Barragan, S.Mir, D.Dzahini (TIMA Lab)

11:00 – 12:00: Session 3 – Posters & Coffee Break

Coordinator: N.-E. Zergainoh

3.1 To Detect or to Correct? A.Bramnik (Intel), Y.Sazeides (U Cyprus)
3.2 A Low-Cost Soft Error Tolerant Read Circuit for Single/Multi-Level RRAM-based Cross-Point RRAM Arrays, H.Bardareh, A.M.Hajisadeghi, H.R.Zarandi (Amirkabir U of Technology)
3.3 A Novel Use of Approximate Circuits to Thwart Hardware Trojan Insertion and Provide Obfuscation, H.Martin, L.Entrera, S.Dupuis, G.DI Natale (U Carlos III de Madrid, LIRMM)
3.4 A Sequentially Untestable Fault Identification Method Based on n-Bit State Cube Justification, T.Hosokawa, M.Niseki, M.Yoshimura, H.Yamazaki, M.Arai, H.Yotsuyanagi, M.Hashizume (Nihon U, Kyoto Sangyo U, Tokushima U)
3.5 On the test of a COTS-based system for space applications, S.Carbonara, A.Firrincieli, M.Sonza Reorda, J.-G.Mess (Politecnico di Torino, German Aerospace Center)
3.6 An Automatic Approach to Perform FMEDA Safety Assessment on Hardware Designs, J.Sini, M.Violante (Politecnico di Torino)
3.7 An Effective Stochastic Number Duplicator and its Evaluations using Composite Arithmetic Circuits, R.Ishikawa, M.Tawada, M.Yanagisawa, N.Togawa (Waseda U)
3.8 Collective-Aware System-on-Chips for Dependable IoT Applications, V.Tenentes, D.Rossi, B.Al-Hashimi (U Southampton, U Hertfordshire)
3.9 Predicting the Impact of Functional Approximation: from Component- to Application-Level, M.Traiola, A.Savino, M.Barbareschi, S.Di Carlo, A.Bosio (LIRMM, Politecnico di Torino, U Naples Federico II)

12:00 – 13:00: Special Session 1 – Low-Power Versus Reliability: A Real Brain-Teaser

Organizer/Moderator: P.Girard (LIRMM)

S1.1 Modern Gain-Cell Memories in Advanced Technologies, E.Amat, R.Canal, A.Rubio (IMB-CNM, UPC)
S1.2 Energy efficiency versus reliability: a (low-power) designer's perspective, A.Garcia-Ortiz (U Bremen)
S1.3 Design Tradeoffs in Bioimplantable Devices: A Case Study with Bladder Pressure Monitoring, S.Mahmud, S.J.A.Majerus, M.S.Damaser, R.Karam (U South Florida, L. Stokes Cleveland Hospital, Lerner Research Inst., Cleveland Clinic Foundation)

13:00 – 14:30: Lunch

14:30 – 15:30: Session 4 – Functional Testing

Moderator: M.Garcia-Valderas (U Carlos III de Madrid)

4.1 Development flow of on-line Software Test Libraries for asynchronous processor cores, A.Floridia, E.Sanchez, N.Andrikos (Politecnico di Torino)
4.2 Fault-Independent Test-Generation for Software-Based Self-Testing, P.Georgiou, X.Kavousianos, R.Cantoro, M.Sonza Reorda (U Ioannina, Politecnico di Torino)
4.3 About the functional test of the GPGPU scheduler, B.Du, J.E.Rodriguez Condia, M.Sonza Reorda, L.Sterpone (Politecnico di Torino)

14:30 – 15:30: Session 5 –System-Level Security

Moderator: S.Di Carlo (Politecnico di Torino)

5.1 Detecting and Resolving Security Violations in Reconfigurable Scan Networks, P.Raiola, M.Kochte, A.Atteya, L.Rodriguez Gomez, H.-J.Wunderlich, B.Becker, M.Sauer (U Freiburg, U Stuttgart)
5.2 Detecting the Existence of Malfunctions in Microcontrollers Utilizing Power Analysis, K.Hasegawa, M.Yanagisawa, N.Togawa (Waseda U)
5.3 Effective Control Flow Integrity Checks for Intrusion Detection, A.Chaudhari, J.Abraham (U Texas at Austin)

15:30 – 15:45: Break

15:45 – 16:45: Special Session 2 – Resistive and Spintronic RAMs: Device, Simulation, and Applications

Organizers/Moderators: E.-I.Vatajelu (TIMA Lab), L.Anghel (TIMA Lab)

S2.1 OxRAM: from Physical Device to Circuit Simulation, J.-M.Portal, M.Bocquet (U Aix-Marseille)
S2.2 STT-MRAM: from Physical Device to Circuit Simulation, G.Prenat (CEA-CNRS, SPINTEC)
S2.3 Storage and Computing based on Resistance-Change Devices, E.-I.Vatajelu, L.Anghel (UGA-TIMA, CNRS)

16:45 – 17:15: Coffee Break

17:15 – 18:15: Special Session 3 – Cross-Layer Fault-Tolerance Under Performance/Power Constraints

Organizer/Moderator: M.Shafique (TU Wien)

S3.1 Hardware and Software Techniques for Heterogeneous Fault-Tolerance, S.Rehman, F.Kriebel, B.S.Prabakaran, F.Khalid, M.Shafique (TU Wien)
S3.2 Efficient Fault Injection for Embedded Systems: As Fast as Possible but as Accurate as Necessary, P.R.Maier, U.Sharif, D.Mueller-Gritschneder, U.Schlichtmann (TU Munich)
S3.3 Power/Area-Optimized Fault Tolerance for Safety Critical Applications, M.Krstic, A.Simevski, M.Ulbricht, S.Weidling (IHP-Microelectronics)
S3.4 Robust co-synthesis of embedded control systems with occasional deadline misses, A.Behrouzian, D.Goswami, T.Basten (TU Eindhoven)

20:00: Welcome Reception

Tuesday July 3, 2018

08:30 – 09:30: Special Session 4 – Neuromorphic Circuits and Systems

Organizer/Moderator: H.Stratigopoulos (LIP6)

S4.1 Event-Driven Bio-Inspired Sensing and Computing Hardware, L.Camuñas-Mesa, B.Linares Barranco (IMS Sevilla)
S4.2 From on-chip self-healing to self-adaptivity in analog/RF ICs: challenges and opportunities, M.Andraud, M.Verhelst (KU Leuven)
S4.3 Error Resilient Neuromorphic Networks Using Checker Neurons, S.Pandey, S.Banerjee, A.Chatterjee (Georgia Tech)

09:30 – 09:45: Break

09:45 – 10:45: Special Session 5 – Aging and Variability

Organizer/Moderator: F.Cacho (ST Microelectronic)

S5.1 CMOS characterization and compact modelling for circuit reliability simulation, J.Diaz Fortuny, J.Martin-Martinez, R.Rodriguez, M.Nafria (U Autònoma de Barcelona), R.Castro-Lopez, E.Roca, F.V.Fernandez (IMSE-CNM, U Sevilla)

S5.2 Reliability Degradations from Physics to CAD, H.Amrouch (Karlsruhe Inst. of Technology)

S5.3 Resistive Switching Behavior seen from the Energy Point of View, J.Gomez, I.Vourkas, A.Abusleme (U Técnica Federico Santa María), A.Rubio (UPC)

10:45 – 11:15: Coffee Break

11:15 – 12:15: Session 6 – Fault Tolerance

Moderator: R.Velazco (TIMA)

6.1 Fault-Resilient Topology Planning and Traffic Configuration for IEEE 802.1Qbv TSN Networks, A.Atallah, G.Bany Hamad, O.Ait Mohamed (Concordia U)

6.2 Self-Stabilizing High-Speed Communication in Multi-Synchronous GALS Architectures, M.Perner, U.Schmid (TU Wien)

6.3 Soft Error Optimization of combinational circuit based on gate sizing and multi-objective particle swarm optimization algorithm, X.Cao, L.Xiao, L.Li, J.Li, J.Li, J.Wang (Harbin Institute of Technology)

11:15 – 12:15: Session 7 – Energy and Variability

Moderator: F.Moll (UPC)

7.1 Minimization of Timing Failures in Pipelined Designs via Path Shaping and Operand Truncation, I.Tsiokanos, L.Mukhanov, D.S.Nikolopoulos, G.Karakonstantis (Queen's U Belfast)

7.2 Independent N-well and P-well Biasing for Minimum Leakage Energy Operation, Y.Okamura, T.Ishihara, H.Onodera (Kyoto U)

7.3 HealthLog Monitor: A Flexible System-Monitoring Linux Service, A.Chatzidimitriou, G.Papadimitriou, D.Gizopoulos (U Athens)

12:15 – 12:30: Break

12:30 – 13:15: IOLTS 2018 Keynote Talk

Rethinking Memory System Design: Robustness, Energy, Performance

O.Mutlu (ETH Zurich and CMU), Moderator: D.Gizopoulos (U Athens)

13:15 – 14:30: Lunch

14:30 – 15:30: Special Session 6 – Special Session 6 - Resolving the Strong Reliability Issues Induced by Multi-Cell Upsets (MCUs) in Memories

Organizer/Moderator: Y.Zorian (Synopsys)

S6.1 Evaluation Tool of MCUs Distributions in Memories, I.Nofal (iRoC)

S6.2 Memory Protection Against MCUs for Advanced Technologies and Automotive Applications, G.Harutunyan (Synopsys)

16:00: Social Event & Dinner

Wednesday July 4, 2018

08:30 – 09:30: Session 8 – Potpourri

Moderator: V.Tenentes (U Southampton)

8.1 Efficient Software-Based Partitioning for Commertial-off-the-Shelf NoC-based MPSoCs for Mixed-Criticality Systems, S.Esposito, S.Avramenko, M.Violante (Politecnico di Torino)

8.2 A Capture Safe Static Test Compaction Method Based on Don't Cares, S.Ochi, H.Yamazaki, T.Hosokawa, M.Yoshimura (Nihon U, Kyoto Sangyo U)

8.3 ESIFT: Efficient System for Error Injection, N.Tian, D.Saab, J.Abraham (CWRU, U Texas at Austin)

08:30 – 09:30: Session 9 – Hardening and Monitoring

Moderator: B.Becker (U Freiburg)

9.1 A New Approach to Threshold Voltage Measurements of Transistors, T.Hillebrand, S.Paul, D.Peters-Drolshagen (U Bremen)

9.2 The case of using CMOS FD-SOI rather than CMOS bulk to harden ICs against laser attacks, J.-M.Dutertre, V.Beroulle, P.Candelier, L.-B.Faber, M.-L.Flottes, P.Gendrier, D.Hely, R.Leveugle, P.Maistri, G.Di Natale, A.Papadimitriou, B.Rouzeyre (CEA-Tech, TIMA, ST Micro, LIRMM, U Grenoble Alpes)

9.3 Emulation of an ASIC Power, Temperature and Aging Monitor System for FPGA Prototyping, A.Listl, D.Mueller-Gritschneder, F.Kluge, U.Schlichtmann (TU Munich)

09:30 – 10:30: Session 10 – Posters & Coffee Break

Coordinator: N.-E. Zergainoh

10.1 Adaptive ECC Techniques for Reliability and Yield Enhancement of Phase Change Memory, S.-K.Lu, H.-P.Li, K.Miyase (National Taiwan U of Science and Technology, Kyushu Inst. of Techn.)

10.2 A Test Register Assignment Method Based on Controller Augmentation to Reduce the Number of Test Patterns, T.Hosokawa, S.Takeda, H.Yamazaki, M.Yoshimura (Nihon U, Kyoto Sangyo U)

10.3 Design and Optimization of Reliable Hardware Accelerators: Leveraging the Advantages of High-Level Synthesis, F.Taher, M.Kishani, B.Carrion Schafer (U Texas at Dallas, Sharif U of Technology)

10.4 DRAM Characterization under Relaxed Refresh Period Considering System Level Effects within a Commodity Server, L.Mukhanov, K.Tovletoglou, D.S.Nikolopoulos, G.Karakonstantis (QUB)

10.5 Finding False Paths for Sequential Circuits Using Operations on ROBDDs, A.Matrosova, S.Ostanin, S.Chernyshov (Tomsk State U)

10.6 Impact of a Laser Pulse on a STT-MRAM Bitcell: Security and Reliability Issues, M.Kharbouche - Harrari, J.Postel-Pellerin, G.Di Pendina, R.Wacquez, D.Aboulkassimi, M.Bocquet, R.Sousa, R.Delattre, J.-M.Portal (CEA, AMU-IM2NP, DRF/INAC/SPINTEC, EMSE)

10.7 Real-Time Validation of Fault-Tolerant Mixed-Criticality Systems, S.Esposito, J.Sini, M.Violante (Politecnico di Torino)

10.8 Reliability Improvements for Multiprocessor Systems by Health-Aware Task Scheduling, R.Schmidt, R.Massoud, J.Raik, A.Garcia-Ortiz, R.Drechsler (U Bremen, TUT)

10.9 Self-healing imager based on detection and conciliation of defective pixels, G.Takam Tchendjou, E.Simeu (TIMA Lab)

10.10 Test Compression Using Extended Nonlinear Binary Codes, O.Novak (TU Liberec)

10:30 – 11:30: Special Session 7 – Robust Design for Smart IoT Systems

Organizer: M.Shafique (TU Wien), Moderator: D. Goswani (TU Eindhoven)

S7.1 Robust Machine Learning Systems: Reliability and Security for Deep Neural Networks, M.A.Hanif, F.Khalid, R.V.Wicaksana Putra, S.Rehman, M.Shafique (TU Wien)

S7.2 Cross-Layer Control Adaptation for Autonomous System Resilience, M.Momtaz, S.Banerjee, S.Pandey, J.A.Abraham, A. Chatterjee (Georgia Tech. and U Texas at Austin)

S7.3 Reliability and Performance Challenges of Ultra-low voltage Caches: A Trade-off Analysis, A.Gebregiorgis, M.Tahoori (Karlsruhe Inst. Technology)

11:30 – 11:45: Break

11:45 – 12:45: Session 11 – Circuit-Level Security

Moderator: D.Rossi (U Hertfordshire)

11.1 Shielding Performance Monitor Counters: a double edged weapon for safety and security, A.Carelli, A.Vallero, S.Di Carlo (Politecnico di Torino)

11.2 Benchmarking the Capabilities and Limitations of SAT Solvers in Defeating Obfuscation Schemes, S.Roshanisefat, H.Thirumala, H.Homayoun, K.Gaj, A.Sasan (George Mason U)

11.3 On the Effect of Aging in Detecting Hardware Trojan Horses with Template Analysis, N.Karimi, J.-L.Danger, S.Guilley (U Maryland Baltimore County, Telecom ParisTech, U Paris-Saclay)

12:45 – 14:00: Lunch

14:00 – 15:00: Special Session 8 – Perspectives and Challenges in Testing Automotive Systems

Organizer/Moderator: P.Bernardi (Politecnico di Torino)

S8.1 Infrastructure-IP for Functional Safety in Automotive SoC, Y.Zorian (Synopsys)

S8.2 Towards an automatic approach for hardware verification according to ISO26262 functional safety standard, J.Sini, M.Sonza Reorda, M.Violante, P.Sarson (Polit. di Torino, Dialog Semicon)

S8.3 Performances VS Reliability: how to exploit Approximate Computing for Safety-Critical applications, G.Rodrigues, F.Kastensmidt, V.Pouget, A.Bosio (LIRMM, UFRGS)

15:00 – 15:15: Symposium Closing Remarks